Title: **IBIS on-board DHS SW Verification and Validation Plan / Acceptance Test Specifications**

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Prepared by: R. Volkmer

Checked by:

Approved by:

Document Change Record

Issue	Date	Sheet	Description of Change
1.0	31.10.99	all	initial issue
1.1	17.2.00		7e,7f,7g new Test cases
1.2			
1.3	8.3.00		Thermal and Electrical tests added
1.4	12.3.00	4.1, 4.2, 4.3, 4.4	Change of requirements for electrical tests, remove of output impedance measurements (some additional explanation added)
	12.3.00	Test case 6j	Spectral timing compression

Table of Contents

1 Introduction

1.1 Scope

This is the test plan for the IBIS Data Handling System (DPE/HEPI). It includes all QM tests at IAAT level (no detectors connected).

1.2 Acronyms

ADD	Architectural Design Document
ADP	Acceptance Data Package
ADR	Architectural Design Review
CSSW	Common Services software
DC	Direct Current
DDD	Detailed Design Document
DDR	Detailed Design Review
DFEE	Digital Front End Electronics
DH	Data Handling
DHS	Data Handling System
DPC	Data Processing Chain
DPE	Data Processing Electronics
ECO	Engineering Change Order
EGSE	Electrical Ground Support Equipment
EID	Experiment Interface Document
EM	Engineering Model
ESA	European Space Agency
FEE	Front End Electronics FM Flight Model
FM	Flight model
FS	Flight Spare model
GRB	Gamma ray burst
HEPI	Hardware Event Pre-processor for IBIS
HK	House keeping
HOOD	Hierarchical Object Oriented Design
IAAT	Institute Astronomie und Astrophysik, Tuebingen, Germany
IAS	Istituto Astrofisica Spazial, Roma
IASW	Integral Application Software
IBIS	Imager on Board of INTEGRAL Satellite
ICD	Interface Control Drawing
ICE	In Circuit Emulator
INTEGRAL	INTErnational Gamma-Ray Astrophysics Laboratory
ISDC	Integral Science Data Centre
ISGRI	Integral Soft Gamma Ray Imager
ISOC	Integral Science Operations Centre
ISSW	Instrument Specific Software
IST	IBIS System Team
ISWT	Integral Science Working Team

MCE	Module Control Electronics
MER	Multiple event reconstruction
MGSE	Mechanical Ground Support Equipment
MOC	Mission Operations Centre
MPE	Module Power Electronics
NA	Not Applicable
OBDH	On-board-Data-Handling-System
OBSW	On-Board Software
PA	Product Assurance
PCB	Printed Circuit Board
PDU	Power Distribution Unit
PICsIT	Pixellated CsI Telescope
PLM	PayLoad Module
PTM	Packet TeleMetry
QA	Quality Assurance
QM	Qualification Model
RBI	Remote Bus Interface
S/C	Spacecraft
SASW	Standard Application Software
SIS	Spacecraft Interface Simulator
SM	Structural Model
SMCT	Service Module Central Tube
SOC	Science Operation Centre
SPU	Scientific Processor Unit
TBC	To Be Confirmed
TBD	To Be Defined
TC	TeleCommand
TM	TeleMetry
VEB	Veto electronic box
VS	Veto Shield

2 Applicable and reference documents

2.1 Applicable documents

AD Nr.	Name	Reference
[AD.01]	Software Project Management Plan for the Data Handling System on board IBIS.	IN.IB.IAS.PL.0025/97 Draft 2 April 1998
[AD.02]	IBIS on-board data management user requirements document	
[AD.03]	ISGRI software User Manual	IN.IB.SAP.RP 0040
[AD.04]	VETO software User Manual	

[AD.05]	IBIS detector unit AIT plan (equals SVVP plan)	TL12159
[AD.07]	PICsIT software user manual	
[AD.08]	IBIS software user manual	
[AD.09]	Test and Verification of HEPI HW and IBIS-IASW	IN-IM-TUB-TN/EL-021
[AD.10]	PICsIT and IBIS TEST Equipments Design Concept	IN-IM-TES-RS-001
[AD.11]	Software Design Document	IN-IM-TUB-SDD-001
[AD.12]	Software Requirement Document	IN-IM-TUB-SRD-001
[AD.13]	HEPI Design Document	IN-IM-TUB-DES-001
[AD.14	HEPI I/F Document	IN-IM-TUB-TN/EL-018
[AD.15]	IBIS Communication Protocol Definition	IN-IM-TUB-ICD-001, Is. 2.4
[AD.16]	HEPI BOARD QM Test description	IN-IM-TUB-TD-01

2.2 Reference documents

RD Nr.	Name	Reference
[RD.1]	Integral Experiment Interface Document - Part A for Instruments	EID-A
[RD.2]	ESA SOFTWARE ENGINEERING STANDARD, ESA-PSS-05-0, Standard to Small software projects	BSSC(96)2
[RD.3]	IBIS Experiment Interface Document - Part C	
[RD.4]	IBIS Configuration Item Data List	IN.IM.IAS.L1.0001/98
[RD.5]	Test and Verification of HEPI HW and IBIS - IASW	IN-IM-TUB-TN/EL-021
[RD.6]	URD Verification Matrix	IN-IM-TUB-VER-001
[RD.7]	HEPI BOARD QM Test description	IN-IM-TUB-TD-01
[RD.8]	HEPI TEST REPORT-Electrical	IN-IM-TUB-TR-01
[RD.9]	HEPI Test Report -Mechanical	IN-IM-TUB-TR-05

3 Description

3.1 Overview

Testing is an activity aimed at :

- Checking software product versus requirements.
- Detecting failures.
- Evaluating the capabilities of the sw system

Four separate test activities have been identified these are
- Test **plan** – Describes the **organisation** behind the testing
- Test **case** specifications – Identifies **what** tests shall be carried out.
- Test **procedure** – Describes **how** the test is performed step by step (for every test case).
- Test **report** – Describes the **results** of each test.

3.2 Test Items

Testing for the Data Handling System at Tübingen is covered in this document. That is:

The CSSW software
The IASW Software
The HEPI
The DPE

3.3 Feature to be tested

All URD requirements should be verified (this could be by inspection, analysis or test).
In RD.6 (URD Verification Matrix) a matrix is shown, which contains the list of requirements to be tested and at which level.

3.4 Features not to be tested

See section 3.3.

3.5 Environmental needs

The test environment and equipment for the different tests is described in RD.5 (Test and Verification of HEPI HW and IBIS - IASW)

3.6 Test Plan

Test Number	Test Item	Where	Environment
QM_01	**Power off to stand-by, Housekeeping and Initialisation**	IAAT	DS, HQM, EM6
QM_02	**Loading/Dumping of IASW / HEPI Tables and Parameters**	IAAT	DS, HQM, EM6
QM_03	**On event messages**	IAAT	DS, HQM, EM6
QM_04	**COMMANDABILITY**	IAAT	DS, HQM, EM6
QM_05	**Diagnostic Mode**	IAAT	DS, HQM, EM6
QM_06a	**Scientific Submode Standard**	IAAT	DS, HQM, EM6
QM_06b	**Scientific Submode Polarimetry**	IAAT	DS, HQM, EM6
QM_06c	**Scientific Submode Photon by Photon**	IAAT	DS, HQM, EM6
QM_06d	**Translation Science Function Tables**	IAAT	DS, HQM, EM6
QM_06e	**CdTe Amplitude Correction and Data Selection**	IAAT	DS, HQM, EM6
QM_06f	**Compton Data Selection**	IAAT	DS, HQM, EM6
QM_06g	**TELEMETRY PRIORITY VIA ICB THRESHOLDS**	IAAT	DS, HQM, EM6
QM_06h	**DUMMY GENERATION AND S8 CELL STATUS**	IAAT	DS, HQM, EM6
QM_06i	**HISTOGRAM COMPRESSION ALGORITHM**	IAAT	DS, HQM, EM6
QM_06j	**SPECTRAL TIMING COMPRESSION**	IAAT	DS, HQM, EM6
QM_07a	**BROADCAST PACKET REACTIONS OF ECLIPSE ENTRY/EXIT**	IAAT	DS, HQM, EM6
QM_07b	**BROADCAST PACKET REACTIONS OF RADIATION BELT ENTRY/EXIT**	IAAT	DS, HQM, EM6
QM_07c	**BROADCAST PACKET REACTIONS ON IREM SETTINGS**	IAAT	DS, HQM, EM6
QM_07d	**BROADCAST PACKET REACTIONS ON IMMINENT SWITCH OFF/ESAM**	IAAT	DS, HQM, EM6
QM_07e	**BROADCAST PACKET REACTIONS ON POINT/SLEW AUTOMATISM**	IAAT	DS, HQM, EM6
QM_07f	**BROADCAST PACKET REACTIONS ON FLAGS ON TARGET AND HAND**	IAAT	DS, HQM, EM6
QM_07g	**BROADCAST PACKET REACTIONS ON ACC FLAG AND AOCS FLAG**	IAAT	DS, HQM, EM6
QM_08	**POWER OFF**	IAAT	DS, HQM, EM6
QM_09	**PATCH/DUMP**	IAAT	DS, HQM, EM6
QM_10	**HEPI Functional tests**	IAAT	DS, DPE-SIM, HQM
QM_13	**Amplitude Correction on HEPI**	IAAT	DS, HQM, EM6
QM_14	**Multiple Event reconstruction on HEPI**	IAAT	DS, HQM, EM6
QM_15	**HEPI Polarimetry on HEPI**	IAAT	DS, HQM, EM6
QM_16	**Spectral Timing on HEPI**	IAAT	DS, HQM, EM6
QM_17	**Histogram Binning on HEPI**	IAAT	DS, HQM, EM6

Test Number	Test Item	Where	Environment
LABEN_F01 (except TC,TM(5,4))	**Transition from Power off to Stand By, Distribution of TC and generation of OEM power off**	LABEN	IS, PI,VE, HQM, EM6
LABEN_F02+ TBD commands	**Context Table Management**	LABEN	IS, PI,VE, HQM, EM6
LABEN_F04+ VETO Spectra	**Scientific Mode Functions + VETO Spectra collection**	LABEN	IS, PI,VE, HQM, EM6
LABEN_F05	**Reactions to Broadcast Packet**	LABEN	IS, PI,VE, HQM, EM6
LABEN_F14	**Noisy Pixel Handling**	LABEN	IS, PI,VE, HQM, EM6
QM_20	**HEPI BOARD ACCEPTANCE TESTS**	ref. below	DS, HQM, EM6
QM21 + QM_20	HEPI Environmental: Electrical I/F	IAAT	DS, HQM, EM6
QM_20	HEPI T/V	INTA	DS, HQM, EM6
QM_20	HEPI Vibration	INTA	DS, HQM, EM6
QM_21	DPE Electrical	IAAT	DS, HQM, EM6
IN-IM-TUB-TR-05	HEPI Mechanical	IAAT	

DS: Detector Simulator; EM5: DPE EM5; EM6: DPE EM6; HQM: HEPI QM; IS: ISGRI QM (MCE3); PI: PICSIT QM (PDM4); VE: VETO QM (TBC)

4 DHS Test description

4.1 Functional tests

An draft overview of the description of applicable tests is given below.

Test Case #1: Power off to stand-by, Housekeeping and Initialisation

- Check the complete initialisation sequence from Off to Stand-By of IASW and HEPI
- Check all kind of HK-packets and the IBIS HK-handling.
- Check all initialisation values of HEPI and IASW.

Note that context loading and verification, as well as LUT load and dump, is not the object of this test case, but it shall be covered in a separate test case (and related test procedures).

Test Case #2: Loading/Dumping of IASW / HEPI Tables and Parameters

This test shall cover the loading and reporting of tables and parameters as defined in both IASW and HEPI.

There will be separate test procedures for instrument context tables of periphery.

For tables and parameters stored in DPE RAM, the following operation shall be tried:
- load from ground
- report from DPE RAM and verification.
- test upload of HEPI register type II from DPE RAM into HEPI
- test upload of HEPI LUT from ground via DPE to HEPI and back.

The translation and upload of the science function tables into HEPI status register is tested in a separate test procedure for science mode tests (QM_???).

Test Case #3:On event messages
This test shall cover the feature of On Event Messages generation, collection and handling.
On event messages are dumped in TM(1, 8) (essential housekeeping H1) in a buffer of 8 messages per telemetry packet.
Only locally by IASW generated OEM shall be tested.
For IASW, only OEM whose generation is possible by means of a well-defined sequence shall be addressed.
Also the feature of OEM overflow in a housekeeping telemetry packet shall be tested.

Test Case #4: COMMANDABILITY
This test provides a frame to verify all possible mode transitions involving Stand by, Diagnostic and Scientific Modes.
The following transitions are identified:
- Stand by --> Diagnostic --> Stand by
- Stand by --> Scientific --> Stand by

Into each operating mode it shall be verified that all (and just) allowed telecommands for that mode are accepted. HK reception shall be verified too.
Table load/report telecommands is covered by test #2.
There will be a test procedure for each operating mode.
The approach to read histograms manually will be tested here.

Test Case #5: Diagnostic Mode
This test shall cover Diagnostic capabilities.
With IASW in Diagnostic Mode and HEPI in Transparent Mode, generation of the following packets shall be verified by this test: transparent packets, ISGRI raw data packets and PICSIT raw data packets.

Test Case #6: Science Mode

Test Case #6a: Scientific Submode Standard
This test shall cover Scientific Submode Standard capabilities.
With IASW/HEPI in scientific submode standard, generation of the following packets shall be verified by this test:
Slew: S1, S2, S3, S4, S5
Pointing: S1, S2, S3, S5, S7, S8
Verify the correct integration times of histograms during pointing-slew-pointing switches.
This test covers not point-slw reaction with BCPK.

Test Case #6b: Scientific Submode Polarimetry
This test shall cover Scientific Submode Polarimetry capabilities.
With IASW/HEPI in scientific submode polarimetry, generation of the following packets shall be verified by this test:
Slew: S1, S2, S3, S4, S5
Pointing: S1, S2, S3, S5, S6, S8
Verify the correct integration times of histograms during pointing-slew-pointing switches.

Test Case #6c: Scientific Submode Photon by Photon
This test shall cover Scientific Submode Photon by Photon capabilities.
With IASW/HEPI in scientific submode photon by photon, generation of the following packets shall be verified by this test:
Slew: S1, S2, S3, S4, S5
Pointing: S1, S2, S3, S4, S5
Verify the correct integration times of histograms.

Test Case #6d: Translation Science Function Tables
This test shall cover the possibilities of the science function tables. For every scientific submode only one scientific function is enabled inside the science function tables.

Test Case #6e: CdTe Amplitude Correction and Data Selection
This test shall cover correct working of CdTe amplitude correction and CdTe PPM data selection.
With IASW/HEPI in scientific submode photon by photon, contents of the S1 packets shall be verified by this test:

Verification of the correct behaviour of photon by photon mode was covered by test QM-06c.

Test Case #6f: Compton Data Selection
This test shall cover correct working of Compton data selection.
With IASW/HEPI in scientific submode photon by photon, contents of the S3 packets shall be verified by this test:

Verification of the correct behaviour of photon by photon mode was covered by test

TEST PROCEDURE #6G: TELEMETRY PRIORITY VIA ICB THRESHOLDS
This test shall cover correct transmitting of scientific TM packets according to their priority set via TM threshold table.
With IASW/HEPI in scientific submode photon by photon the scientific functions S1-S5 are tested.
With IASW/HEPI in scientific submode standard the scientific functions S7 and S8 are tested.
With IASW/HEPI in scientific submode polarimetry the scientific function S6 is tested.
With IASW/HEPI in diagnostic/transparent modethe scientific functions S13.1-3 and report tasks parameter TM packets are tested.

Verification of the correct behaviour of modes were covered by test QM-05 + QM06A-C.

TEST PROCEDURE #6H: DUMMY GENERATION AND S8 CELL STATUS
This test shall cover the reconstruction of 32 bit time information inside scientific TM S1, S3, S4 and the cell status switch of S8 from 2 active cells to 8 active cells with IASW/HEPI in scientific submode standard.
This test covers not point-slew reaction with BCPK, correct working of the mode is verified in test procedures QM6A-C.

TEST PROCEDURE #6I: HISTOGRAM COMPRESSION ALGORITHM
This test shall cover the correct working of the histogram compression algorithm inside scientific TM S5, S6, S7.0 and S7.1.
This test covers not point-slew reaction with BCPK, correct working of the mode is verified in test procedures QM6A-C.

TEST PROCEDURE #6J: SPECTRAL TIMING HISTOGRAM COMPRESSION ALGORITHM
This test shall cover the correct working of the histogram compression algorithm inside scientific TM S8
This test covers not point-slew reaction with BCPK, correct working of the mode is verified in test procedures QM6A-C.

Test Case #7: BROADCAST PACKET REACTIONS

Test Case #7a: BROADCAST PACKET REACTIONS OF ECLIPSE ENTRY/EXIT
This test procedure shall verify IASW reactions to eclipse event. This covers time comparison of eclipse time in the BCPK, end of running science mode and context save/restore facility.

Test Case #7b: BROADCAST PACKET REACTIONS OF RADIATION BELT ENTRY/EXIT
This test procedure shall verify IASW reactions to radiation belt event. This covers time comparison of radiation belt time in the BCPK and end of running science mode.

Test Case #7c: BROADCAST PACKET REACTIONS ON IREM SETTINGS
This test procedure shall verify IASW reactions to high radiation report in BCPK.

TEST CASE #7D BROADCAST PACKET REACTIONS ON IMMINENT SWITCH OFF/ESAM
This test procedure shall verify IASW reactions to ESAM field and Imminent switch off field report in BCPK.

TEST CASE #7E: BROADCAST PACKET REACTIONS ON POINT/SLEW AUTOMATISM
This test procedure shall verify IASW reactions on BCPK for pointing duration and pointing ID. Especially the behaviour of the science histogram handling shall be verified.

TEST CASE #7F: BROADCAST PACKET REACTIONS ON FLAGS ON TARGET AND HAND OVER
This test procedure shall verify IASW reactions for BCPK on-target flag and hand over flag.

Especially the behaviour of the science histogram handling shall be verified.

TEST CASE #7G: BROADCAST PACKET REACTIONS ON ACC FLAG AND AOCS FLAG
This test procedure shall verify IASW reactions for BCPK on-ACC current mode and AOCS submodes.
Especially the behaviour of the science histogram handling shall be verified.

Test Case #8: POWER OFF
This test procedure shall verify IASW power off sequence as driven by TC from ground.

TEST CASE #9: PATCH/DUMP
This test procedure shall verify that IASW may be changed via patch commands and checked via dump commands.
Patch shall be verified by replacing the S7 histogram compression algorithm with different one which was used in the IBIS IASW EM campaign (compression of cells containing values below 15 into singe nibble).
Dump shall be verified by reading the version number.

Test Case #10: HEPI Functional tests
This test case covers the HEPI functionality which requires the DPE Simulator. This includes

- Verification of all HEPI commands
- CsI Energy selection on HEPI
- Detection of time coincidence of CdTe and CsI events on HEPI
- Multiple event Reconstruction
- Testing of CsI Rate Meters
- Generation of on event messages
- Set and clear registers and error flags on HEPI

Test Case #11: N/A

Test Case #12: N/A

Test Case #13: Amplitude Correction on HEPI
Test the CsI amplitude correction on HEPI with different LUT and input files.

Test Case #14: Multiple Event reconstruction on HEPI
Check multi-event reconstruction overflow flag (with DPE).

Test Case #15: HEPI Polarimetry on HEPI
This test should verify the proper processing of PICSIT CsI double events which have adjacent pixel locations by HEPI. These events should be recognized to contain polarimetry information reported in the polarimetry histogram.

Test Case #16: Spectral Timing on HEPI

The test should verify for HEPI the proper handling of the spectral timing facility which will collect periodically in different energy channels all incomming CsI events. The setting of energy channels could be changed which will also be verified with this test.

Test Case #17: Histogram Binning on HEPI
This test should verify that the mapping of the HEPI histogram LUT for all histograms distributes the energy in the proper channels.

TEST PROCEDURE #18: N/A

TEST PROCEDURE #19: N/A

TEST PROCEDURE #20: HEPI BOARD ACCEPTANCE TESTS
Check the functionality and PCB of the HEPI board for incomming/outgoing inspection and during acceptance tests (T/V; etc.) Check of complete initialisation sequence; transparent, histogram and PPM modes.

4.2 Environmental tests

The description of the environmental tests of the HEPI board is given in RD.7 (HEPI BOARD QM Test description)

4.3 Electrical tests

4.3.1 Power interface

Parameters:

- Overall power consumption measured at the unit input
- HEPI overall peak power consumption (duration should be less than 2 sec)
- Input current
    - Inrush current transition
    - Inrush current duration

IMPORTANT NOTE: DURING all tests, the HEPI must be connected with the DPE 4 MHz clock !!!

4.3.1.1 Power Consumption in nominal mode

Measure the current at the input of the unit by means of a multimeter being the unit in running (science date processing) state. This measure will be performed at 4.75V, 5V and 5.25V.
Acceptance criteria (current): < 200 mA

4.3.1.2 Power Consumption in stand by mode

Measure the current at the input of the unit by means of a multimeter being the unit in stand by state (no data transmission). This measure will be performed at 4.75V, 5V and 5.25V.
Acceptance criteria (current): < 180 mA

4.3.1.3 Power Consumption in initialisation mode

Measure the current at the input of the unit by means of a multimeter being the unit during initialisation. This measure will be performed at 4.75V, 5V and 5.25V.
Acceptance criteria (current): < 250 mA

4.3.1.4 Load current transition HEPI stand alone

Record with a scope the inrush current transition at the power up of the unit.
Inrush current duration <= 5 msec

4.3.1.5 Load current transition HEPI in DPE spare slot

Record with a scope the inrush current transition (primary voltage) at the power up of the DPE with and without HEPI.
Inrush current duration <= (TBD) msec

Accuracy
Voltage: +/- 3 % oscilloscope, +/-0.5% digital multimeter

4.3.2 Serial lines interface

4.3.2.1 Parameters:

- Serial lines
  - Waveform and timing characteristics
  - Data transmitted and quiescent state in output lines
- Low speed serial output lines: output voltage corresponding to high level and low level, communication protocol specification
- Low speed serial input lines: input voltage corresponding to high level and low level communication protocol specification
- High speed serial lines: output voltage corresponding to high level and low level
- High speed serial input lines: input voltage corresponding to high level and low level, input impedance
- Fault voltage tolerances, common mode input voltages, output impedance and short current to ground will **not** be verified by measurements (but control of the implemented design). The required design from EID-A to the I/F is also verified by impedance measurements (input only) and voltage levels. Short current measurements are not applied because of to much the stress of the QM/FS.

4.3.2.2 Specification: RD.1, AD.13, AD.14, AD.15

4.3.2.3 Low speed serial lines

4.3.2.3.1 Output lines

4.3.2.3.1.1 Waveform characteristics

Monitoring of following lines (with break out box):
LBR Clock, Data Return
Send a command from DPE to HEPI for data request (e.g. HK)
Verify following parameters:
Transfer of data:

- preparation of new data on the data channel at the falling edge of the clock
- Stabilisation of the new data at the rising edge of the clock
- Check that bit ”0” corresponds to low level voltage
- Check that bit ”1” corresponds to high level voltage
- Delay between end of transmission of 8 bits and start of transmission of the next one included in the same block
- Delay from end of HK request reception by HEPI from DPE and HK block transmission by HEPI to DPE

Data signal period T=61.03 usec

4.3.2.3.1.2 Electrical measurements

- Check that the quiescent state of the data return line shall be the transmission of bit ”1”
- Measure the differential output voltage with the scope of the data return line

4.3.2.3.2 Input Lines

4.3.2.3.2.1 Waveform characteristics

Monitoring of following lines (with break out box):
LBR Clock, Data Forward
Send a message to HEPI (e.g. HK request)
Verify following parameters
Transfer of data:

- preparation of new data on the data channel at the falling edge of the clock
- Stabilisation of the new data at the rising edge of the clock
- Check that bit ”0” corresponds to low level voltage
- Check that bit ”1” corresponds to high level voltage
- Delay between end of transmission of 8 bits and start of transmission of the next one included in the same block
- Time gap between two successive commands

4.3.2.3.2.2 Electrical measurements

- Measure the differential input voltage

- Measure the input impedance from input to ground

4.3.2.4 High speed lines (HEPI – DPE)

4.3.2.4.1 Waveform characteristics

Connect a break out box in the serial line connector in order to monitor the following signals by scope:

- Clock HBR A, RX_DATA_A, Enable_A
- Clock HBR B, RX_DATA_B, Enable_B

Select line A:

Start the generation of input data for HEPI. Send a command to start the transmission of data HBR A. Record the waveform of the new data on the data channel at the falling edge of the clock and verify following parameters

- Preparation of the new data after receipt of the enable line low signal and falling edge of the clock
- Stabilisation of the data at the rising edge of the clock
- check that data bit ”1” corresponds to high level line
- check that data bit ”0” corresponds to low level line

Repeat with line B.

4.3.2.4.2 Electrical measurements

4.3.2.4.2.1 Output lines

- Measure the output voltage with a scope of the data line

4.3.2.4.2.2 Input lines

- Measure the input voltage with a scope in the clock and enable lines
- Measure the differential input impedance
- Measure input impedance from input to ground

4.3.2.5 High speed lines (Detectors – HEPI)

4.3.2.5.1 Waveform characteristics

Connect a break out box in the serial line connector in order to monitor the following signals by scope:

- CSI DATA, CSI FIFO IIE, SAMPLE CSI, GEII CLK CSI, SYIIC CSI, CLR FIFO CSI
- CDTE DATA, CDTE FIFO IIE, SAMPLE CDTE, GEII CLK CDTE, SYIIC CDTE, CLR FIFO CDTE

Select line CsI I/F:

Go with DPE in diagnostic mode. Initialise HEPI. Start the generation of input data for HEPI. Record the waveform of the new data on the data channel at the falling edge of the clock and verify following parameters

1. Preparation of the new data after receipt of the sample line low signal and falling edge of the clock and FIFO NE is low
2. Stabilisation of the data at the rising edge of the clock
3. check that data bit ”1” corresponds to high level line
4. check that data bit ”0” corresponds to low level line
5. send a reset command and verify that the clear FIFO line goes low for a short time (238 nsec)
6. check that the synchronisation pulse is provided each 2 sec (238nsec active low)
7. check the delay between synchronisation pulse and BCP 2 is less than 1120 nsec.
8. Send a command to program the delay to additional 5 cycles
9. check the delay between synchronisation pulse and BCP 2 is now 1190 nsec larger then in step 7

Repeat with CdTe I/F.

- send a reset command to HEPI
- check that the delay between SYNC CSI and SYNC CDTE is less then 50 nsec

4.3.2.5.2 Electrical measurements

4.3.2.5.2.1 Output lines

- Measure the output voltage with a scope of the clock, Clear FIFO, Synchronisation and sample lines

4.3.2.5.2.2 Input lines

- Measure the input voltage with a scope in the data and FIFO NE lines

4.3.2.6 Acceptance criteria

4.3.2.6.1 Low speed lines

Data signal period

T=61.03usec

Output lines characteristics

Differential output voltage	Low level	-6V to -2V
	High level	+2 V to +6V

Input lines characteristics

Differential input voltage	Low level	-6V to -0.4V
	High level	+0.4 V to +6V

4.3.2.6.2 High speed lines (HEPI – DPE)

Data signal period
T= 190 nsec

Output lines characteristics

Differential output voltage	Low level	-6V to -2V
	High level	+2 V to +6V

Input lines characteristics

Differential input voltage	Low level	-6V to -1V
	High level	+1 V to +6V
Differential input impedance	120 Ohm +/- 5%	

Input impedance from input to ground TBD (about 800 Ohm)

4.3.2.6.3 High speed lines (HEPI – Detectors)

TBW

4.3.3 mRTU I/F

4.3.3.1.1 Parameters

4.3.3.1.1.1 On/Off command lines

- Pulse voltage and width
- output voltage rise and fall times

4.3.3.1.1.2 Relay switch status channel

- current
- voltage

4.3.3.2 Specification: RD.1

4.3.3.3 Method and Acceptance criteria

4.3.3.3.1 On/off command lines

Send relay commands and verify that the active level is 12 to 16 V and 13msec +/-2msec width to the HEPI reset line.
The pulses will be monitored by means of a scope, at the same time the fall and rise times will be measured. They shall be <= 500usec. The current should not exceed 180 mA at 14V

4.3.3.3.2 Relay switch status channel

Verify that the high state threshold of the HBR A and B request lines is above 3.6 V.
Generate data on the HBR A and B I/F but don't read them out.
Verify that the low state threshold of the HBR A and B request line is below 1 V and the contact current is less than 10 mA.

4.3.3.4 Timing I/F

4.3.3.4.1 Parameters

BCPs 2: This pulse are provided at a frequency of 1 Hz

Synchronisation Clock: This clock provides a frequency of 4 MHz

Heart beat: This clock provides a 1 Hz clock generated from the 4 MHz and BCP 2.

4.3.3.4.2 Specifications

RD.1

4.3.3.4.3 Methods and Acceptance criteria

4.3.3.4.3.1 Electrical characteristics

BCP and synchronisation clock:
Verify with a scope the following levels
High level: +2 V to +6 V
Low level: –2 V to –6 V
Rise/fall times: < 20 nsec

Verify the input impedance is 120 +/– 10 Ohm.

Heart beat:
Verify that the high state threshold of the heart beat line is above 3.6 V.
Verify that the low state threshold of the heart beat line is line is below 1 V and the contact current is less than 10 mA.

4.3.3.4.3.2 Timing characteristics

Synchronisation clock: The frequency shall be 4.194304 MHz
BCP 2: Using a scope to measure that the pulses have a width of 1.9 usec (negative level) with a puls repetition frequency of 1 Hz.
Heart Beat: 1 Hz with 1 sec low and 1 sec high states

4.4 Environmental Test

4.4.1 Thermal Vacuum

(Ref. AD.16)

4.4.2 Thermal Tests

This test is to verify the electrical characteristics at different temperatures and will be performed at IAAT. This tests will be performed with the HEPI connected to the DPE but mounted in a test frame. This test frame will be put into a Thermal box. Only active output signals will be measured, because DPE is not within the box.
Additional small functional tests will be applied on different input voltages of the power supply (4.6 and 5.5V) on the maximum and minimum operating temperature.
Maximum operating temperature: 70
Minimum operating temperature: -30

- Complete functional and electrical tests prior to the temperature cycling
- The equipment shall be put into a frame into the temperature chamber
- The control of the temperature of the unit will be performed near the position of the ASIC on the PCB
- Perform initial electrical and functional test at ambient temperature
  - The equipment is switched off and the temperature is decreased and stabilised at the low non operating minimum temperature (TNO-min) during the time t_E. (T= –35°C qualification). The temperature is increased at the low operating level (TQ-min=–30°C) This temperature is maintained to switch the equipment on. After a time t_E, the electrical test is performed.
  - The temperatue increased up to the high non operating level (TNO-max). (T=75°C qualification).
  - After a dwell time T_E the temperature is decreased to the hot start-up level (TSU-high) to switch ON the equipment and the temperature is maintained at the high operating temperature (TQ-max=TSU-high) during a time t_E . After the time t_E the electrical test is performed. (T=70 °C qualification).

The cycling is finished performing a final reduced electrical and functional test at ambient temperature.

4.5 Mechanical tests

The description of mechanical tests of the HEPI is given in RD.9 (HEPI Test Report -Mechanical) This document must be updated.