Title: **HEPI BOARD QM Test description**

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1 Introduction

1.1 Scope

The document describes the HEPI QM Board qualification tests.
Parts of the tests will be applied at CRISA (Madrid) and parts at IAAT (Tübingen).

1.2 Acronyms

CSSW	Common Services Software
DC	Direct Current
DFEE	Digital Front End Electronics
DH	Data Handling
DPE	Data Processing Electronics
EGSE	Electrical Ground Support Equipment
EID	Experiment Interface Document
EM	Engineering Model
FEE	Front End Electronics FM Flight Model
FM	Flight model
FS	Flight Spare model
GRB	Gamma ray burst
HEPI	Hardware Event Pre-processor of IBIS
HK	House keeping
IASW	Integral Application Software
IBIS	Imager on Board of INTEGRAL Satellite
ICD	Interface Control Drawing
INTEGRAL	INTErnational Gamma-Ray Astrophysics Laboratory
ISDC	Integral Science Data Centre
ISGRI	CdTe layer
ISOC	Integral Science Operations Centre
ISSW	Instrument Specific Software
ISWT	Integral Science Working Team
MOC	Mission Operations Centre
MCE	Module Control Electronics
MER	Multiple event reconstruction
MGSE	Mechanical Ground Support Equipment
MPE	Module Power Electronics
OBDH	On-Board Data Handling
OBSW	On-Board Software
PCB	Printed Circuit Board
PICSIT	CsI layer
PDU	Power Distribution Unit
PLM	PayLoad Module
PTM	Packet TeleMetry
QM	Qualification Model
RBI	Remote Bus Interface

SASW	Standard Application Software
S/C	Spacecraft
SIS	Spacecraft Interface Simulator
SM	Structural Model
SMCT	Service Module Central Tube
SOC	Science Operation Centre
SPU	Scientific Processor Unit
TBC	To Be Confirmed
TBD	To Be Defined
TC	TeleCommand
TM	TeleMetry
VEB	Veto electronic box
VS	Veto Shield

1.3 Applicable and reference documents

1.3.1 Applicable documents

AD.1: EID-A rev 5
AD.2: DPE HW Design Description, INT-DD-CRS-0001, Is.1
AD 3: URD, Is.3 draft, August 1999

1.3.2 Reference documents

RD 1: HEPI Interface Description, IN-IM-TUB-TN/EL-018, Is. 4.1
RD 2: HEPI Design Description, IN-IM-TUB-DES-001, Is 5.1
RD 3: IBIS FM Electrical ICD, TL 13282, Is. 5

HEPI Harness and detector description, IN-IM-TUB-TN/EL-017

RD : Software I/F Control Document, INT-IC-GMV-0001 Is. 3
RD : Integral Packet structure Definition, INT-RP-AI-0030, Is.04
RD : IASW SDD, IN-IM-TUB-SDD-001, Is. 1
RD : IBIS UM, Is. 3
RD : The Onboard Compton selection, IN-IB-SAP-RP-045; 9/1998
RD : IBIS Communication Protocol Definition, IN-IM-TUB-ICD-01, Is. 1

1.4 HEPI Board description

The HEPI board consists out of two PCB mounted on an frame. This frame is normally mounted within the DPE Spare slot.
A more detailed description is given in RD 1 and RD 2.

2 General Conditions

2.1 Environment

Thermal tests for verification of the electronic levels at different temperatures shall performed at IAAT on the clean bench.
Vibration tests and Thermal vacuum test shall performed at CRISA.

2.2 Test equipment

2.2.1 Tests at IAAT

Following test equipment is required for the tests at IAAT:
1. SIS
2. OBDH FE
3. DPE EM 6
4. Detector Simulator
5. Thermal Box

All tests at IAAT shall be performed with HEPI in the Thermal Box at low pressure (< 2mbar) and within the required temperature range .

2.2.2 Test at CRISA

Following test equipment is required for the tests at CRISA:
1. SIS
2. OBDH
3. DPE EM 6
4. Detector simulator
5. Thermal vacuum chamber
6. vibration desk

2.3 Test harness

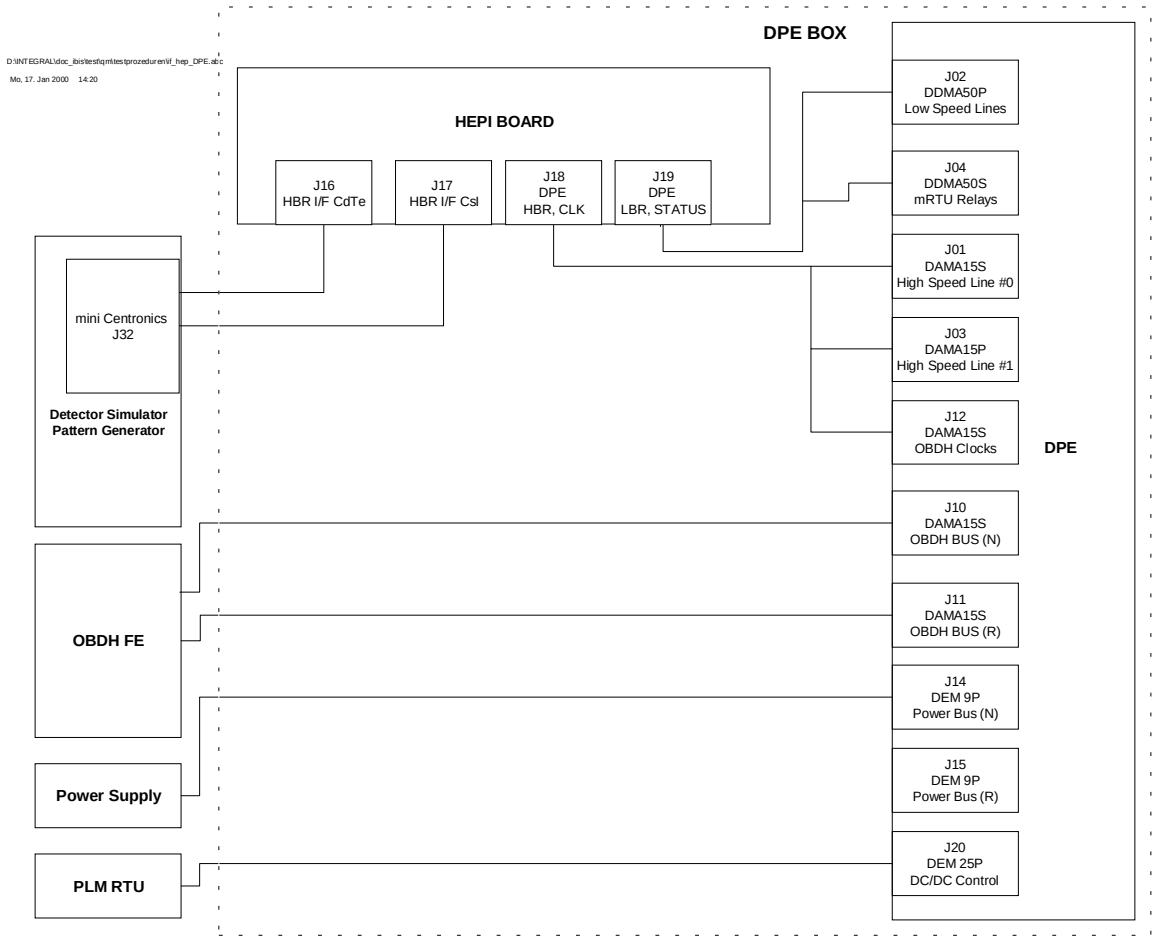


Figure 1: Conncections of HEPI Board Test environment

2.3.1 IAAT

The harness outside the Thermal box is a standard EM one. Only the connection between OBDH and DPE (different rooms) is 5 meter.

2.3.2 CRISA

The harness during vibration tests shall be the standard EM harness from ALENIA.
For the T/V tests a modified detector simulator harness is required. The harness description is given in Chapter 3.

2.4 Tests verification

For testing the functionality of the board the test procedure QM_20 will be applied. This procedure is able to test the functionality of all HW of the HEPI board.
The verification of the test results could be either done on the SIS and OBDH or on an external workstation.

The output of the SIS archive shall be processed by a program named „TM_ENC„. This encoder separate the TM packets from the SIS archive file according their APID.
After each test run the output shall be compared with a reference output.

2.4.1 Sinusoidal and Vibration

2.4.1.1 Parameters

The equipment shall withstand sinusoidal and randam vibration due to the excitations of the launcher.

2.4.1.2 Specification

RD.1

2.4.1.3 Qualification

1. Perform a visual inspection to check the appearance of the unit before vibration
2. Perform a reduced functional and electrical test
3. Perform a resonance search of the empty fixture, verifying that no resonance appear from 5Hz to 2000Hz.
4. Perform sinusoidal and random vibration to check that the levels are correct
5. Mount the equipment to a fixture through the normal mounting points of the equipment (Axis x).
6. Perform a resonance search of the test fixture and the test item, a low level sine vibration 0.5g) shall be performed in this interval 5-2000 Hz at 2 octave per minute.
7. Performa a sinusoidal qualification test, sweep up and down at 2 octave per minute, according to the below described figure:

Frequency (Hz)	Level
5 – 18	+/– 11mm
22,5 - 100	+/– 22.5g

8. Perform another resonance search of the test fixture and the item as previously defined to verify that the equipment has withstood the vibration test.
9. Perform a random qualification test, with 2 minutes duration according to the below described figure:

Frequency (Hz)	Level
20 – 100	+6dB/Octave
100 – 500	0.1 g^2/Hz
500 – 2000	– 6dB/octave

10. Perform another resonance search of the test fixture and the item as previously defined to verify that the equipment has withstood the vibration test.

11. Perform a reduced functional and electrical test to check that the equipment has survived the vibration test.

Repeat step 3, 4, 5, 6, 7, 8, 9, 10 and 11 with axis Y and Z.

2.4.2 Shock

2.4.2.1 Parameters

Capability of the equipment to withstand the separation level pyrotechnic shock induced by the separation of the payload from the launcher.

2.4.2.2 Specification

RD.1

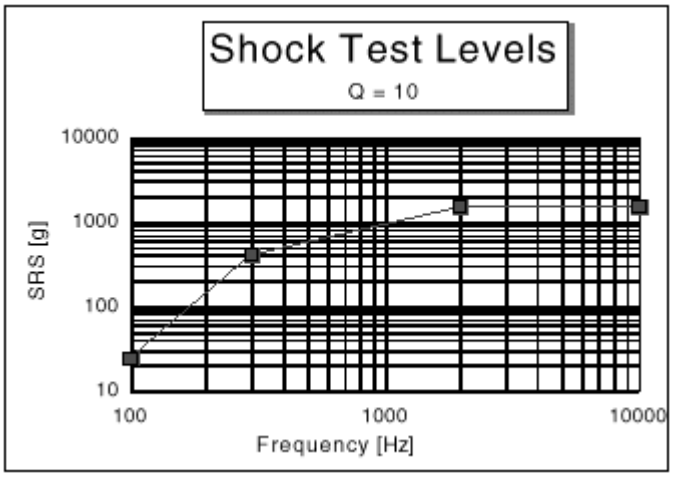
2.4.2.3 Method

1. Perform a visual inspection to check the appearance of the unit before vibration
2. The unit will be mounted to a fixture through its normal attachment points
3. Apply shock transient on axis X

(B. Vinai)

Frequency [Hz]	SRS-Acceleration[g]
100	
100-300	
300	
300-2000	
2000-10000	25
rising slope	
400	
rising slope	
1500	

EID-A + DPE:



4. Perform a visual inspection, a reduced functional and electrical check to verify that the equipment has withstand the shock.

2.4.2.4 Acceptance criteria

No damage has been occurred to the equipment after application of the transient shocks. Measured parameters during the reduced electrical and functional tests shall be within the tolerances.

2.4.2.5 Vacuum temperature cycling

2.4.2.5.1 Parameters

Ability of the equipment to perform in a thermal vacuum environment which simulates the acceptance temperature limits for the equipment increased or decreased by the qualification margin of 5°C and the test set-up tolerances.

2.4.2.5.2 Specification

RD.1

Maximum non-operating temperature:	65
Maximum operating temperature:	50
Minimum non-operating temperature:	-35
Minimum operating temperature:	-30
Number of cycles:	8

2.4.2.5.3 Method

Qualification and acceptance thermal vacuum tests

- Complete functional and electrical tests prior to the vacuum temperature cycling
- The equipment shall be boltered to a representative mounting panel using the correct bolts and bolts torques
- The mounting panel shall be black painted (except the mounting contact area) and have the length and the width of the DPE with a thickness of a standard platform/sidewalls
- The control of the temperature of the unit will be performed in the temperature reference point defined in the Interface Control Drawing.
- Perform initial electrical and functional test at ambient temperature
- Qualification thermal vacuum cycling will be as described:
  - The temperatue is increased first, up to the high non operating level (TNO-max). (T=60 ° acceptance and T=65°C qualification). The pressure will be decreased up to 1.3 10^{-5}.
  - After a dwell time T_E the temperature is decreased to the hot start-up level (TSU-high) to switch ON the equipment and the temperature is maintained at the high operating temperature (TQ-max=TSU-high) during a time t_E . After the time t_E the functional test is performed. (T=45 °C acceptance, 50 °C qualification).
  - The equipment is switched off and the temperature is decreased and stabilised at the low non operating minimum temperature (TNO-min) during the time t_E. (T=–30°C acceptance, –35°C qualification). The temperature is increased at the low operating level

(TQ-min). This temperature is maintained to switch the equipment on. After a time t_E, the functional test is performed.

- Next cycles consists in increasing temperature to the high operating level and after a time t_E, a (reduced) functional test, then decrease the temperature to the low operating temperature and after a time t_E perform (reduced) functional tests.
- The cycling is finished performing a final functional test at ambient temperature.

3 Harness

3.1 Harness between Detector Simulator and HEPI Board

The next table describes the harness between detector simulator and HEPI board.

DCMA 37 S	Detector Simulator	DET_SIM_J32		Note (2)	Type	Towards:		
Pin. No.	Interface name	Line description	Line name			Equipment	connector	Pin No(1)
1	Det. HBA I/F CsI	CsI Sample	SAM_CSI+	TP 1,2		HEPI	J17	3
2	Det. HBA I/F CsI	CsI Sample Return	SAM_CSI+			HEPI	J17	12
3	Det. HBA I/F CdTe	CdTe synch.	SYNC_CDTE+	TP 23,24		HEPI	J16	5
4	Det. HBA I/F CdTe	CdTe synch. Return	SYNC_CDTE-			HEPI	J16	14
5	Det. HBA I/F CsI	CLOCK CSI	CLK_CSI+	TP 7,8		HEPI	J17	4
6	Det. HBA I/F CsI	CLOCK CSI Return	CLK_CSI-			HEPI	J17	13
7	Det. HBA I/F CdTe	CLOCK CDTE	CLK_CDTE+	TP 9,10		HEPI	J16	4
8	Det. HBA I/F CdTe	CLOCK CDTE Return	CLK_CDTE-			HEPI	J16	13
9	Det. HBA I/F CdTe	CdTe Sample	SAM_CDTE+	TP 15,16		HEPI	J16	3
10	Det. HBA I/F CdTe	CdTe Sample Return	SAM_CDTE-			HEPI	J16	12
11	NC							
12	NC							
13	NC							
14	NC							
15	Det. HBA I/F CdTe	CdTe Clear FIFO	CLR_FIFO_CDTE+	TP 25,26		HEPI	J16	6
16	Det. HBA I/F CdTe	CdTe Clear FIFO Return	CLR_FIFO_CDTE-			HEPI	J16	15
17	Det. HBA I/F CsI	CsI Clear FIFO	CLR_FIFO_CSI+	TP 27,28		HEPI	J17	6
18	Det. HBA I/F CsI	CsI Clear FIFO Return	CLR_FIFO_CSI-			HEPI	J17	15

DCMA 37 S	Detector Simulator	DET_SIM_J32		Note (2)	Type	Towards:		
Pin. No.	Interface name	Line description	Line name			Equipment	connector	Pin No(1)
19	Det. HBA I/F CdTe	CdTE Data out	CDTE_DT+	TP 37,38		HEPI	J16	1
20	Det. HBA I/F CdTe	CdTE Data out Return	CDTE_DT-			HEPI	J16	10
21	Det. HBA I/F CsI	CsI FIFO Not empty	CSI_FIFO_NE+	TP 39,40		HEPI	J17	2
22	Det. HBA I/F CsI	CsI FIFO Not empty Return	CSI_FIFO_NE-			HEPI	J17	11
23	Det. HBA I/F CdTe	CdTE FIFO Not empty	CDTE_FIFO_NE+	TP 43,44		HEPI	J16	2
24	Det. HBA I/F CdTe	CdTE FIFO Not empty Return	CDTE_FIFO_NE-			HEPI	J16	11
25	Det. HBA I/F CsI	CsI Data out	CsI_DT+	TP 45,46		HEPI	J17	1
26	Det. HBA I/F CsI	CsI Data out Return	CsI_DT-			HEPI	J17	10
27	NC							
28	NC							
29	NC							
30	NC							
31	NC							
32	NC							
33	NC							
34	NC							
35	NC							
36	NC							
37	NC							

3.2 Harness HEPI DPE

Connector Name:	HEPI HIGH SPEED LINES	HEPI_J18 (DPEXXYYYJ18)		Note		Type	Towards:		
Pin. No	Interface name	Line description	Line name				Equipment	connector	Pin No

Connector Name:	HEPI HIGH SPEED LINES	HEPI_J18 (DPEXXYYYJ18)		Note		Type	Towards:		
Pin. No	Interface name	Line description	Line name				Equipment	connector	Pin No
1	Fast serial line A	Data Line A	DTHA+	TP 1,10		HBA	DPE	J01	4
10		Data A (compl.)	DTHA-			HBA	DPE	J01	5
2		Clock A	CLKHA+	TP 2,11		HBA	DPE	J01	2
11		Clock A (compl.)	CLKHA-			HBA	DPE	J01	3
3		Enable A	ENHA+	TP 3,12		HBA	DPE	J01	6
12		Enable A (compl.)	ENHA-			HBA	DPE	J01	7
4	Fast serial line B	Data Line B	DTHB+	TP 4,13		HBA	DPE	J03	4
13		Data Line B (compl.)	DTHB-			HBA	DPE	J03	5
5		Clock HBA B	CLKHB+	TP 5,14		HBA	DPE	J03	2
14		Clock B (compl.)	CLKHB-			HBA	DPE	J03	3
6		Enable B	ENHB+	TP 6,15		HBA	DPE	J03	6
15		Enable B (compl.)	ENHB-			HBA	DPE	J03	7
7	On Board Clock BUS	General sync.	BCP2+	TP 7,16		HBA	DPE	J12	5
16		General sync. (compl.)	BCP2-			HBA	DPE	J12	13
8		General Clock	GEN_CLK+	TP 8,17		HBA	DPE	J12	9
17		General Clock (compl.)	GEN_CLK-			HBA	DPE	J12	2
9		NC							
19		NC							
18		NC							
20		NC							
21		NC							
22		NC							
23		NC							
24		NC							
25		NC							

Connector Name:	HEPI HIGH SPEED LINES	HEPI_J18 (DPEXXYYYJ18)		Note		Type	Towards:		
Pin. No	Interface name	Line description	Line name				Equipment	connector	Pin No
26		NC							

Connector Name:	HEPI LOW SPEED LINE	HEPI_J19 (DPEXXYYYJ19)		Note		Type	Towards:		
Pin. No	Interface name	Line description	Line name				Equipment	connector	Pin No
1	Slow serial line	Clock	CLK+	TP 1,10		LBA	DPE	J02	5
10		Clock (compl.)	CLK-			LBA	DPE	J02	38
2		Data Forward	DTF+	TP 2,11		LBA	DPE	J02	1
11		Data Forw. (compl)	DTF-			LBA	DPE	J02	18
3		Data return	DTR+	TP 3,12		LBA	DPE	J02	2
12		Data return (compl)	DTR-			LBA	DPE	J02	19
18		Init HEPI (DPE Relay pulse 7)	INIT+	TP 18,26		On/off	DPE	J04	9
26		Init HEPI (compl.)	INIT-			On/off	DPE	J04	25
19		Chassis		common shield					
20	(mRTU)	Request line A+ (Relay Status 0)	ROHA+	TP 20,21		Opto	DPE	J04	11
21		Request line A (compl.)	ROHA-			Opto	DPE	J04	27
22	(mRTU)	Request line B+ (Relay Status 1)	ROHB+	TP 22,23		Opto	DPE	J04	12
23		Request line B (compl.)	ROHB-			Opto	DPE	J04	28
24		HEPI Status+ (Relay Status 2)	BA+	TP 24,25		Opto	DPE	J04	13

Connector Name:	HEPI LOW SPEED LINE	HEPI_J19 (DPEXXYYYJ19)		Note		Type	Towards:		
Pin. No	Interface name	Line description	Line name				Equipment	connector	Pin No
25		HEPI Status-	BA-			Opto	DPE	J04	29
4		NC							
5		NC							
6		NC							
7		NC							
8		NC							
9		NC							
13		NC							
14		NC							
15		NC							
16		NC							
17		NC							
20		NC							
21		NC							
22		NC							
23		NC							
24		NC							
25		NC							