Title: **HEPI Design Report**

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Document Change Record

Issue	Date	Sheet	Description of Change
Draft 0.1	1st July, 1996	all	First issue of the document
Draft 0	Dec. 1996	all	
1.0	Jan. 1997	all	typos
2.0	Febr. 1997	8	mechanical dimensions
		17	data types
		21	overview of the electronic design
		28-29	spectral timing (new)
		29	size of pre-burst buffer
		30	burst buffer (new)
		33-34	power allocation (new)
3.0 draft	August 97	9	mechanically interfaces
		14	distribution of timing synchronisation
		15	timing of HBR I/F HEPI – DPE
		16	data format HBR I/F A
		17	data format HBR I/F B
		18	LBR I/F
		22	Loadable parameters
		22	Loadable thresholds
		23	Control register
		24	data register
		28	detailed design
		29	multiple event reconstruction
		30	histogram
		38	Burst detection
		39	rate meters
		40	Energy selection
3.0	September 97	13	Timing HEPI, detectors
		22	HEPI control register
		23	LUT organisation
		26	Main memory organisation
4.0	November 97	14	Scheme of HBR I/F
		21	Data modes
			HEPI control register
			Main Memory organisation
			Accumulation CsI events (histogram)
			Burst detection deleted
			Rate meters
5.0 draft	January 98		Status Register
			Memory organisation
	March		Control Register
			Error Register

Issue	Date	Sheet	Description of Change
5.1	June	14	Timing scheme of HBR I/F
		22	HEPI data flow overview
		25	Coding scheme of CsI polarimetry events
		31	HEPI PCB
6.2 draft	August	14	Table 1: Description of EHPI commands
		18	Status and Control bits of HEPI changed
		26	Figure 8 updated
		27, 28, 29	Figure 9,10,11 include: HEPI data paths
		30	Energy correction. Additional explanations
		31	Multiple event reconstruction: Add. Explanations and constraints
		32	Polarimetry: Pixel identification table changed
		34	Time coincidence detection: Add. Explanations
		35	Accumulation: Add. Explanations, Memory mapping
		36	Spectral timing: Add. Explanations, Constraints
		38	Energy selection: Add. Explanations
6.2		All	Typos
6.3		35	Memory Mapping
		21	Default settings Register type II
6.4		28	Energy correction +/- offset
		17	HEPI Status Register
		35	Time coincidence with calibration events
		35	Time coincidence switch off
		31	MP transparent
6.5	October	12	Description of distribution of timing information
		15	Description of commands
		17	Description of memory organisation
		20	Description of type II register
6.6	January 2000	5.1.2	Error Register
		4.1.3.1, 4.1.3.2	HBR Description
		7.11	Heart beat
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1 Introduction

1.1 Scope

This report documents the current status for the HEPI (Hardware Event Pre-processor of IBIS) assembly, the data preprocessing unit of the DPE (Data Processing Electronics) of the IBIS instrument.

1.2 Acronyms

CSSW	Common Services Software
DC	Direct Current
DFEE	Digital Front End Electronics
DH	Data Handling
DPE	Data Processing Electronics
EGSE	Electrical Ground Support Equipment
EID	Experiment Interface Document
EM	Engineering Model
FEE	Front End Electronics FM Flight Model
FM	Flight model
FS	Flight Spare model
GRB	Gamma ray burst
HEPI	Hardware Event Pre-processor of IBIS
HK	House keeping
IASW	Integral Application Software
IBIS	Imager on Board of INTEGRAL Satellite
ICD	Interface Control Drawing
INTEGRAL	INTErnational Gamma-Ray Astrophysics Laboratory
ISDC	Integral Science Data Centre
ISGRI	CdTe layer
ISOC	Integral Science Operations Centre
ISSW	Instrument Specific Software
ISWT	Integral Science Working Team
MOC	Mission Operations Centre
MCE	Module Control Electronics
MER	Multiple event reconstruction
MGSE	Mechanical Ground Support Equipment
MPE	Module Power Electronics
OBDH	On-Board Data Handling
OBSW	On-Board Software
PCB	Printed Circuit Board
PICSIT	CsI layer
PDU	Power Distribution Unit
PLM	PayLoad Module
PTM	Packet TeleMetry
QM	Qualification Model
RBI	Remote Bus Interface

SASW	Standard Application Software
S/C	Spacecraft
SIS	Spacecraft Interface Simulator
SM	Structural Model
SMCT	Service Module Central Tube
SOC	Science Operation Centre
SPU	Scientific Processor Unit
TBC	To Be Confirmed
TBD	To Be Defined
TC	TeleCommand
TM	TeleMetry
VEB	Veto electronic box
VS	Veto Shield

2 Applicable and reference documents

2.1 Applicable documents

AD.1: EID-A rev5
AD.2: DPE HW Design Description, INT-DD-CRS-0001,Is.1

2.2 Reference documents

RD 1: HEPI Interface Description, IN-IM-TUB-TN/EL-018, IS. 4.1
RD 2: IBIS Communication Protocol Definition, IN-IM-TUB-ICD-01, Is. 1

3 Description

3.1 Overview

HEPI is the interface between the detector plane and the DPE. The events, which are generated at the CdTe layer (ISGRI) and the CsI layer (PICSIT), are pre-processed and some of them are accumulated in histograms. Each detector layer consists of eight modules. A FIFO Data Manager (FDM) for each detector collects the digital output data of these modules and sorts them by time. HEPI gets the data via an unidirectional High bit rate serial interface (HBR I/F) from each detector. The control of these HBR I/F's is done by the HEPI. After pre-processing and accumulating the DPE reads out the data also via a HBR I/F. This interface is controlled by the DPE. Controlling and exchanging of HK and look up table data is intended via a serial, bi-directional Low Bit Rate Interface (LBR I/F). The DPE processes the data and hands them over to the On Board Data Handling system (OBDH).
The HEPI electronics will be built up with ASICSs for the QM/FM. For the EM we will use FPGAs for high flexibility of the development.

3.2 System characteristics

Clock frequency	4,194,304 Hz
time resolution of the detectors	238.4 nsec within 2 sec
time resolution of the HEPI	61.04 µsec within 72.8 h
HBR I/Fs detectors to HEPI:	
max. theor. data transmission of each I/F	65,536 events/sec ∗ 64 bit event **4,194,304 bit/sec**
expected data rate from ISGRI [A]	1220 events/sec ∗ 64 bit/event **78,080 bit/sec**
expected data rate from PICSIT	2,000 to 25,000 events/sec∗64 bit/event **1,600,000 bit/sec**
Total input to HEPI	**1,678,080 bit/sec**
HEPI to DPE	
max. theor. data transmission	5242880 bit/sec
expected data rate HBR I/F A:	
CdTe Photon by photon	980 events/sec ∗ 80 bit/event 78,400 bit/sec
Compton	240 events/sec ∗ 160 bit/event 38,400 bit/sec
CsI photon by photon (spectral timing, 1ms)	1,024 events/sec ∗ 160 bit/event 163,840 bit/sec

[A] potential higher during on ground calibration

total A **280,640 bit/sec**

expected data rate HBR I/F B:
histograms 2,359,296 byte
8 byte header / 1992 byte 9475 byte
transmission time 1300 sec

total B **14,577 bit/sec**

Total expected data rate between HEPI and DPE **295,217 bit/sec**

4 Interfaces

4.1 Electrical interfaces

4.1.1 High bit rate interface: HEPI - detectors

The fast serial line interface transmits scientific data from the detectors to the HEPI in only one direction. Synchronisation information is transmitted to the detectors from HEPI.
It consists of six differential twisted lines:

- data (from detector)
- sample (from HEPI)
- FIFO not empty (from detector)
- clock (from HEPI)
- synchronisation (from HEPI)
- clear FIFO (from HEPI)

These six lines control the data transmission and timing via hardware handshaking. The clock frequency is 4,194,304 Hz and should be synchronous to the system clock.
Each HBR I/F counts the number of incoming events.
The length of each transmitted word is 64 bit and consists of four 16 bit sub words.

1st word: Time in units of 238.4 ns (most significant 16 bit of 24 bit time word)
2nd word: 8 bit Time (least significant 8 bit of 24 bit time word) plus
8 bit Rise Time (only applicable for CdTe)
3rd word: 12 bit Amplitude (CdTe 11 bit, CsI 10 bit) plus 1 bit flag for CdTe Calibration or plus 1 bit flags for CsI calibration, 1 bit multiple module, 2 bit pulse ID and 2 bit multiplicity (1,2 or 3 events)
4th word: Pixel Address (CdTe 14 bits, CsI 12 bits)
The pixel address of the individual pixel is: Y value (6 bit for CsI or 7 bit for CdTe) and Z value (6 bit for CsI or 7 bit for CdTe).

The data are right adjustified, where applicable. The LSB of information is the LSB of a 16 bit word. The transmitted sequence of the words is 1,2,3,4. The MSB is transmitted first.

1st word

MSB															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
time 1st byte (MSB)								time 2nd byte							

2nd word

16	17	18	19	20	21	22	23	24	25	260	271	282	29	30	31
time 3rd byte (LSB)								rise time (only CdTe)							

3rd word

32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
cal. flag					amplitude (CdTe)										
cal. flag	mmc	pulse ID		MUX	amplitude (CsI)										

4th word

															LSB
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
		address (CdTe)													
				address (CsI)											

Figure 1: Format of data packages from the detectors to HEPI (mmc: multiple module coincidence, MUX: Multiplicity)

4.1.1.1 Timing of the data transmission of the HBR I/F between the detectors and HEPI

If the FIFO_not_empty line is high HEPI generates the sample pulse on the falling edge of the clock pulse to get the next data word. On the next rising edge of the clock pulse [1] (the numbers corresponds to Figure 2) the source (IFDM or PFDM) writes a new data word from the detector FIFO to the output shift register. Due to the propagation delay of the lines and the drivers the clock pulse at the detector is delayed between 8 and 60 nsec. This is also true of the data, i.e. the first data is after max. 60 nsec at the HEPI input register. If the data word was the last data word in the output FIFO the FIFO_not_empty [FIFO NE] line should go low within the next 7.6 micro sec.

On the next rising edge of the clock pulse [2] HEPI shifts one bit from the RS 422 receiver to the input shift register (HEPI gets DATA-new-1). At this time the output register shifts the next bit to the RS 422 driver. Then, on the next rising edge [3] HEPI shifts this bit into its input register and so on.

If the FIFO_not_empty line is still high and HEPI is also ready for read in, HEPI generates a new sample pulse with the falling edge of the 64th clock pulse from the beginning. With the next rising edge [65] HEPI reads the last bit (64th) of the previous data word in and the source writes the next data word to the output shift register and the transmission continues. With the

next falling [65] edge of the clock pulse, i.e. after complete a transmission of one data word (64 bit), HEPI reads the data from the input shift register.
If the FIFO_not_empty line is not high, HEPI generates no new sample pulse and reads only the data word from the input shift register.

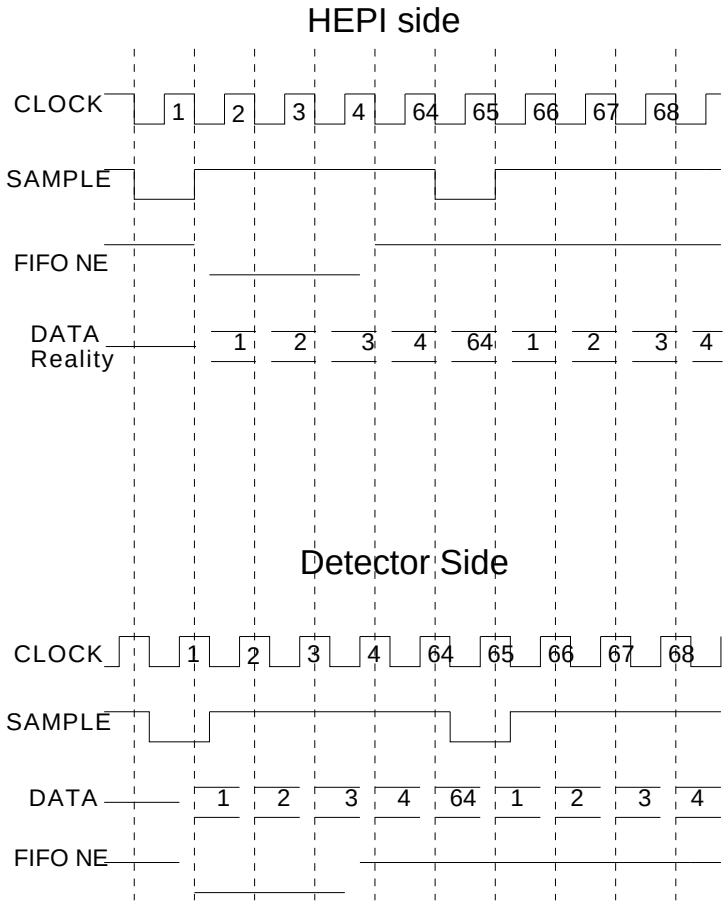

Figure 2: Timing scheme of HBR I/F between detectors and HEPI

4.1.1.2 Distribution of timing and synchronisation information

For timing and synchronisation purposes the DPE generates and distributes a 4,194,304 Hz and an 1 sec pulse clock (BCP 2) with 1.9 µsec pulse width..
From the 1 sec pulse HEPI generates synchronisation pulses with a 2 sec time period. The timing is shown in (Figure 3). The sync-line goes low with the rising edge of the clock (plus internal propagation delays). The pulse width of the HEPI generated sync pulse is one clock cycle (238 nsec).
To compensate the delay of each detector electronics this pulse is individually delayed and distributed to ISGRI and PICSIT and resets every 2 sec the detector time counters.

4.1.2 Starting and timing of an observation cycle

For starting the observation the DPE generates just after a BCP 2 (about the time t_{n-1}) a dedicated telecommand (start synchronisation) to synchronise the detectors. The time of the next BCP 2 is stored in DPE and distributed with additional HK to ground. At t_n (cf. Figure 3) HEPI generates a new synchronisation pulse. Together with the clear detector FIFO signals they are individually delayed and distributed to the detectors with the rising edge of the clock pulse.. The time counters of the detectors are set to 0 with the synchronisation pulse. The active low signal of the clear FIFO line clear the output FIFOs of the detectors.
The pulse width of the FIFO clear pulse is one DPE clock cycle (234 nsec).
The time difference between t_n and t_{n-1} is 1 sec (one BCP 2 period).
The detectors fill their output FIFOs with newly measured events and mark them with a time tag with 238 nsec time resolution within 2 sec (23 bit). HEPI reads them out and looks for time coincidences between the two detector layers.
Then the last 8 bit of the time information are cut off and 17 bit additional time information is added to the time field. The resulting time resolution is 61.035 µsec within 72.8 h (32 bit).
With this time information the events are handed over to the DPE. The DPE puts the event with this time resolution into the TM packages.

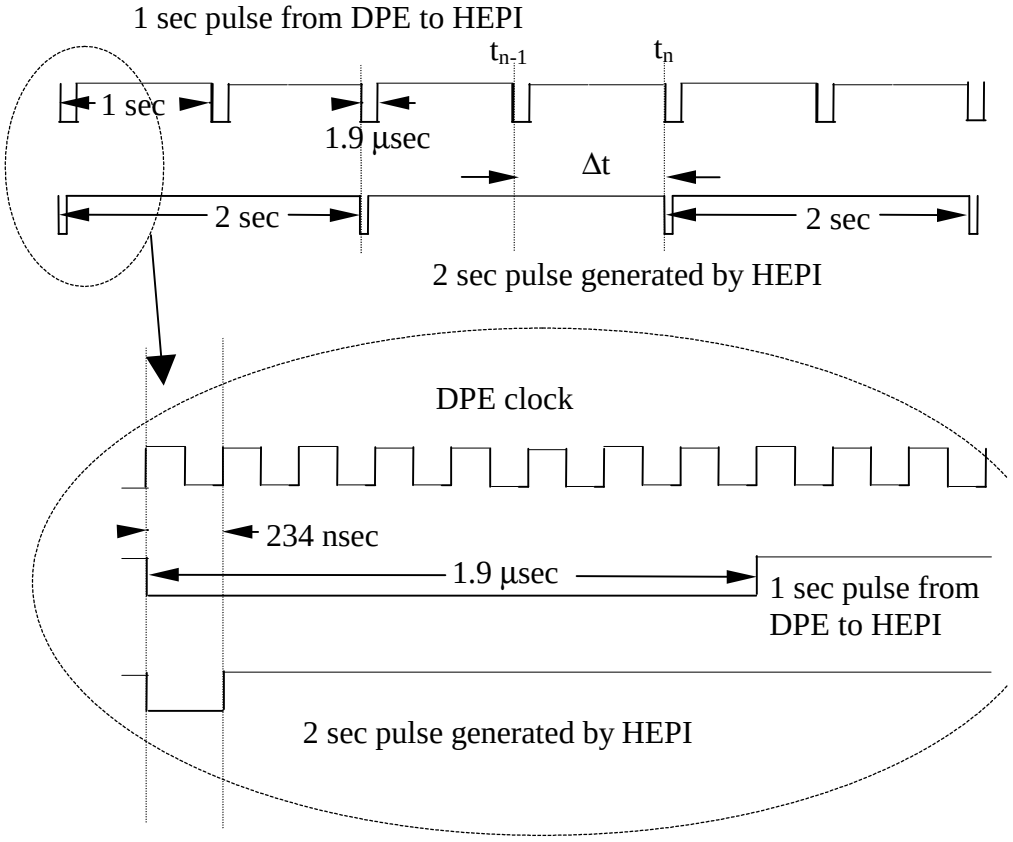

Figure 3: Timing and synchronisation scheme from HEPI and DPE

4.1.2.1 HEPI commanding scheme

The DPE/IASW controls HEPI with commands transmitted via the LBR I/F. The command syntax is described in RD 1.

4.1.2.1.1 Initialisation of HEPI

After power up all registers (cf. 5.1.1 and 5.1.2) within the HEPI are set to zero, HEPI works automatically within the diagnostic mode and after a TBD time HEPI is ready for receiving commands.
The DPE/IASW SW could also initialise a hardware reset via INIT HEPI line.

4.1.2.1.2 Receiving commands

After initialisation HEPI is ready to receive commands.
Each incoming command is counted by the RECEIVED COMMAND COUNTER. The counter counts the incoming valid commands.
The transmission starts, when HEPI detects the start bit of the transmitted word.
HEPI checks the incoming parity bit. If the check is wrong, the complete data are rejected and the REJECTED COMMAND COUNTER is increased.
The on event message counter of the HK packet is increased by one and the on event message field is filled according RD 1.

The time between adjacent commands is larger than 1 msec.

CID	Description
001	Init HEPI: Clears all HEPI Register Clears Main Memory from address 16#000 to 16# 480 000 Clears LUT RAM (CsI rate meter) from address 16#000 to 16 # 2000 This requires about 4 sec. Clears HEPI HBR A FIFO and HBR B FIFO Clears CsI Detector FIFO and CdTe detector FIFO Set default values for all internal type II register. As a result HEPI goes in transparent mode. After receipt of this command HEPI start to clear the main memory and in parallel the CsI rate metes. This requires
002	Clears HEPI HBR A FIFO and HBR B FIFO Clears CsI Detector FIFO and CdTe detector FIFO Set default values for internal type IIall register. As a result HEPI goes in transparent mode. This command is similar as 001 but without clear of the external Memory (LUT and main).
003	Set the HEPI status register with the programmable values.
004	Read the HEPI status register. After receipt HEPI read the internal status register (24 bit) and send this information via LBR I/F to DPE (total 6 byte will be send)
009	Set LUT RAM via LBR I/F with programmable values. After receipt HEPI writes the transmitted LUT parameters from start_address to start_addrss + 127 into the LUT RAM. The science data processing is not stopped during this upload (internal RNE-signal is running).
010	Read LUT RAM via LBR I/F from start to start+128-1. After receipt HEPI read the content of the LUT RAM from start address to start address +127 and send it to DPE (data format ref. RD1). The addresses are given in bytes. The science

	data processing is not stopped during this process (internal RNE-signal is running).
012	Read the contents of the main memory. After receipt HEPI reads out the main memory (CsI histograms) from address start*1024 to start*1024+1023. The address is given in kbyte (start_addrsss*1024). The contents is put into the output FIFO of the HBR I/F B (data format ref. RD1).The science data processing is not stopped during this process (internal RNE-signal is running).
013	Clear Counter and Register within HEPI). After receipt HEPI clears the internal register and counter according the bit mask given in RD 1 Table 2.
079	Start synchronisation with next synch. pulse. After receipt HEPI clears **in parallel** with the next synchronisation pulse coming from the DPE: HEPI HBR A FIFO andbut not HBR B FIFO and set default values for internal type IIall register. CsI Detector FIFO and CdTe detector FIFO will be cleared with individually delay and synchronous with the sync pulse. As a result HEPI goes in transparent mode. This command is used to synchronises the CsI detector and the CdTe detector. All events with an old time information are deleted (also on the detector but not in FIFO HRB B to DPE).
117	Read register type II. After receipt HEPI read the content of the type II register and send the contents to DPE (data format ref. RD1).
118	Read standard HK. After receipt HEPI generates a HK data block (data format ref. RD1).
121	Set register type II. After receipt HEPI set the register type II (32 byte) with programmable values.
122	Clear ratemeters. After receipt HEPI clears the LUT RAM from address 16#000 to 16 # 2000 (CsI rate meters). The science data processing is not stopped during this process (internal RNE-signal is running).
124	Clear Memory from start to stop address. After receipt HEPI clears the main memory RAM (CsI histograms) from start address to stop address.. The science data processing is not stopped during this process (internal RNE-signal is running).

Table 1: HEPI command description

4.1.3 High bit rate interfaces: HEPI – DPE

HEPI will transmit the scientific data via two HBR I/Fs to the DPE. These two interfaces are different from the one between the detectors and HEPI.
They consist of four lines:

- data (from HEPI)
- enable (from DPE)
- clock (from DPE)
- request (from HEPI to mRTU)

The length of each transmitted character is 16 bit. Each output FIFO of HEPI is 8 kword. The clock frequency is 5 MHz.
The electrical definitions are in agreement with AD.1 and AD2.
The request lines are connected with the mRTU (relay status).
Table 2 shows an example of an timing scheme of the HBR I/F. Two data words are transmitted. Due to the late high tx_enable signal at each end of a transmission two additional bits of the next word are transmitted. Because the transmission of the accompanying data word is not finished, this data word must be stored and re-transmitted in the next transmission cycle. The output FIFOs could be reset via a dedicated command from DPE-IASW or during initialisation of HEPI.

Signal	DPE-Side (nsec)		HEPI side (nsec)	
tx_enable ↓	0	0	60 (propagation delay)	60

Signal	DPE-Side (nsec)		HEPI side (nsec)	
detection of tx_enable ↓			60 + 95 (half period) [clock ↑]	155
1st bit on line	60 (prop. delay) + 310	370	155 +95 (half period) + 60 (internal delay) [clock↓]	310
sample of 1 bit (b)	2.5 clock cycles after tx_enable	475		
2nd bit on line	60 (prop.) + 500	560	120+ 2*190 (period)	500
sample of 2nd bit	3.5 clock cycles after tx_enable	665		
…	…		…	
16th bit on line	60 (prop.) + 3160	3220	120 + 16*190	3160
sample of 16th bit	17.5 clock cycles after tx_enable	3325		
Reading the output FIFO and loading the shift register with the 2nd data word			60 + 17*190	3230
1st bit of the 2nd data word on the line			60 (internal delay) + 3230	3290
FIFO_WRN	18 clock cycles after tx_enable	3420		
Reading the output FIFO and loading the shift register with the 3rd data word			60 + 33*190	6270
1st bit of the 3rd data word on the line			60 (internal delay) + 3290	6330
FIFO_WRN	34 clock cycles after tx_enable	6460		
tx_enable ↑	34 clock cycles after tx_enable	6460	60 (prop.) + 6460	6520
shift of the 2nd bit of 3rd word to the output			60 + 34*190	6520
detection of tx_enable↑			60+6460+90 (half period) [clock ↑]	6615
stop of transmission				6615

Table 2: Timing scheme of HBR I/F

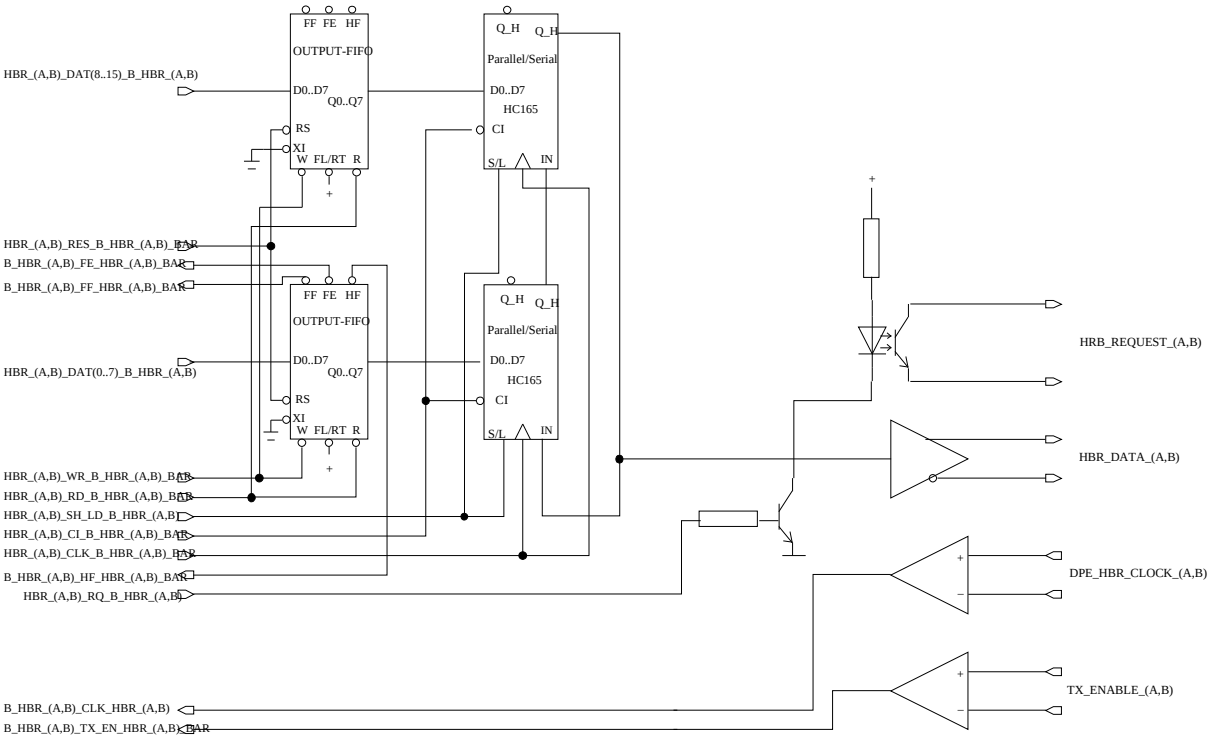

Figure 4: Scheme of HBR I/F HEPI - DPE

4.1.3.1 HBR I/F A

The HBR I/F A will be used to transmit the events, which are not stored inside the HEPI (e.g. photon by photon) and HBR I/F B will be used to readout the histograms.
This requires different definitions of the data packages for these two lines.
HBR I/F A uses two different package sizes: one short (80 bit) and one long (160 bit). The field definition depends on the event type, but in any case starts with the type field (8 bit). Each value inside the data package is right adjustified.
Before transmission, the output FIFO of HBR A must be filled with events. If the number of bytes exceeded the programmable threshold (999 word), the HBR A request lines goes low. The DPE polls this line and will read the data, one block with 1000 word, if required by the IASW data processing.

4.1.3.2 HBR I/F B

HBR I/F B transmits the content of the mass memory (except the LUT).
HEPI put the data from the memory from start-address to stop-address after a DPE-IASW command to the line. Start-address and stop-address are parameters of the command.
If the number of words exceed the programmable threshold (512 word) the request line goes low. The DPE polls this line and will read the data, one block with 512 word, if required by the IASW data processing.

5 Data types at HEPI and DPE Data modes

Different data modes of the IMAGER are intended.
The following list identifies tasks which are done by HEPI and/or DPE:

Task No	Description	HEPI (H), DPE (D)
0	acquire data from CsI and CdTe detector layers through two HBR I/Fs	H
1.	Detection of time coincidence between CdTe and CsI events, apart of calibration events	H
2.	Synchronising time information	H
3.	Amplitude correction of CsI events	H
4.	Reconstruction of CsI multiple events	H
5.	Energy selection CsI single, multiple	H
6.	Pseudo Photon by Photon mode (CdTe and CsI events)	D,H
7.	Histogram of CsI single events	H
8.	Histogram of CsI multiple events	H
9.	Histogram of CsI calibration events	H
10.	Histogram of CsI polarimetry events	H
11.	Toggle buffer to read out the histograms	H
12.	Spectral timing	H
13.	CsI rate meters	H
14.	Collecting of house keeping (HK) data	D
15.	Data compression	D
16.	Telemetry of scientific data	D
17.	Telemetry of HK data	D
18.	Controlling and monitoring of the detectors, VEB and HEPI	D
19.	Distribution of telecommands	D
20.	Transparent modes	H,D

Table 3: List of HEPI and DPE processes

A more detailed description of these tasks is given in the On Board Data processing URD, the Software URD and the HEPI URD.

5.1 Loadable parameters of HEPI

To get a high flexibility of HEPI all thresholds and LUTs of the different data processes are programmable from the DPE. The following list shows this in detail.
The LUT are stored inside a RAM outside the ASIC. The thresholds and control registers are stored direct on the FPGA/ASIC registers.
The data of these registers and LUT can be read out via the LBR I/F with dedicated telecommands from the IASW.
All data registers (internal registers in ASIC) of HEPI are set to default values after reset pulse on the init line, reset command, synchronisation or init command via LBR I/F.
The LUT could be set with individual values by a dedicated command via LBR I/F and set to default values from init command via LBR I/F. A lower part of the LUT RAM is used as individually pixel rate meters of PICSIT detector.

5.1.1 HEPI control and status register

Table 4 lists the status bits of the control register.
After initialisation of HEPI all control register values will be set to zero.

Bit number	Description	Value (0/1)	Modul	DTrans-parent	Std-Poin.	Slew & PPM	Pol-Poin.
1.	CdTe HBR I/F detector - HEPI	ON/OFF	CDTE_HBR	0/1	0	0	0
2.	CsI HBR I/F detector - HEPI	ON/OFF	CSI_HBR	0/1	0	0	0
3.	Amplitude correction	OFF/ON	AC	0	1	1	1
4.	Rate meters	OFF/ON	LUT	0	1	1	1
5.	Multiple event reconstruction	OFF /ON	MP	0	1	1	1
6.	Only for tests used (LBR I/F disable time out)	ON/OFF	LBR	0	0	0	0
7.	CsI spectral timing	OFF/ON	SPT	0	1	0	1
8.	CsI Energy selection+PPM	OFF/ON	ES,HBR_A	0	0	1	0
9.	Spare			0	0	0	0
10.	CsI Calibration event histogram	OFF/ON	HIST	0	1	1	1
11.	CsI single/multiple event histogram	OFF/ON	HIST	0	1/0	0	0
12.	Only for tests used (HBR HF FIFO flag)	OFF/ON	HBR	0	0	0	0
13.	Status Polarimetry histogram	OFF/ON	HIST	0	0	0	1
14.	Time coincidence module	OFF /ON	TC	0	1	1	1
15.	Disable compton detection	OFF /ON	TC	0	0	0	0
16.	Spare			0	0	0	0
17.	Spare			0	0	0	0
18.	CdTe PPM	OFF/ON	HBR_A	0	1	1	1
19.	Only used for Tests (On event message Built in test)			0	0	0	0
20.	CsI sing./mult. histogram Memory Area	I/II	HIST	0	0/1	-	0/1
21.	CsI cal. histogram Memory Area	I/II	HIST	0	0/1	0/1	0/1
22.	Spare			0	0	0	0
23.	Spare			0	0	0	0
24.	Spare			0	0	0	0
25.	Spare			0	0	0	0

Table 4: Status and control bits of HEPI (included in HK data packet)

The control registers could be read out after a dedicated DPE-IASW command (part of essential HK).

5.1.2 HEPI data register

Table 5 shows the content of data registers type HK (counter and flags). These registers could be read out via a dedicated DPE-IASW command (part of essential HK data).

Register	Description	MODUL	Range	Access

number				
1.	Counter CsI events	CSI_HBR	MSByte	R
2.	Counter CsI events	CSI_HBR	3rd byte	R
3.	Counter CsI events	CSI_HBR	2nd byte	R
4.	Counter CsI events	CSI_HBR	LSByte	R
5.	Counter CdTe events	CDTE_HBR	MSByte	R
6.	Counter CdTe events	CDTE_HBR	3rd byte	R
7.	Counter CdTe events	CDTE_HBR	2nd byte	R
8.	Counter CdTe events	CDTE_HBR	LSByte	R
9.	number of CsI events > 10 MeV	MP	MSByte	R
10.	number of CsI events > 10 MeV	MP	LSByte	R
11.	Zerocrossing counter CdTe events	TC	MSBit	R
12.	Zerocrossing counter CdTe events	TC	Bit 15 .. 8	R
13.	Zerocrossing counter CdTe events	TC	LSByte (Bit 7..0)	R
14.	Zerocrossing counter CsI events	TC	MSBit	R
15.	Zerocrossing counter CsI events	TC	Bit 15 .. 8	R
16.	Zerocrossing counter CsI events	TC	LSByte (Bit 7..0)	R
17.	Number of received commands	LBR		R
18.	Number of requests	LBR		R
19.	Number of rejected commands	LBR		R
20.	Last command	LBR		R
21.	Error Register I	(ref. Table 6)		R
22.	Spare			
23.	Spare			

Table 5: Data registers type HK (included in HK data packet)

An error or overflow in on of the modules of HEPI rises a flag in the corresponding error register (ref. **Table 6**). The description of the different flags is listed in Table 6. All error flags could be set to 0 individually by command with CID 13 or general by reset, synchronisation and init command.

Bit Number of Error (Reg. 21, **Table 5**)	Modul	Error condition
0	AC	Amplitude correction (overflow of multiplication and addition, underflow of subtraction)
1	LUT	Ratemeters overflow (more then 64535 number of events in one ratemeter cell)
2	MEM	Error overflow histogram (more then 254 number of events in one histogram cell)
3	SPT	Spectral timing overflow . (more then 254 number of events in one histogram cell)
4	TC	Overflow counter zerocrossing CsI events (more then 2^24 -1 wrap over of the 2 sec period. Overflow of zerocrossing counter of CdTe events is not monitored, because both counters could only differ by one digit because of the synchronisation of the detectors
5	MP	Overflow counter of CsI events >10 MeV (more then 2^16 -1 events with more then 10 MeV after last synchronisation, reset,

		init or clear)
6	CDTE_HBR	Overflow counter CdTe events (more then 2^32 -1 number of events after from last synchronisation, reset, init or clear)
7	CSI_HBR	Overflow counter CsI events (more then 2^32 -1number of events after last synchronisation, reset, init or clear)

Table 6: HEPI Error Flags

Table 7 shows the register with loadable parameters (HEPI type II registers) . These parameters could also be readout via LSL with a dedicated command.

Byte number	Description	MODUL	default value after HEPI reset	Range	Access
0.	MER threshold of double events	MP	0	MSB ... MSB-7	R/W
1.	MER threshold upper threshold of triple events	MP	0	MSB ... MSB-7	R/W
2.	MER threshold lower threshold of triple events	MP	0	MSB ... MSB-7	R/W
3.	Spectral timing integration time	SPT	0	0.9 ... 500 msec	R/W
4.	Spectral timing upper threshold (9)	SPT	0	MSB ... MSB-7	R/W
5.	Spectral timing threshold 8	SPT	0	MSB ... MSB-7	R/W
6.	Spectral timing threshold 7	SPT	0	MSB ... MSB-7	R/W
7.	Spectral timing threshold 6	SPT	0	MSB ... MSB-7	R/W
8.	Spectral timing threshold 5	SPT	0	MSB ... MSB-7	R/W
9.	Spectral timing threshold 4	SPT	0	MSB ... MSB-7	R/W
10.	Spectral timing threshold 3	SPT	0	MSB ... MSB-7	R/W
11.	Spectral timing threshold 2	SPT	0	MSB ... MSB-7	R/W
12.	Spectral timing lower threshold (1)	SPT	0	MSB ... MSB-7	R/W
13.	Energy selection lower threshold	ES	0	MSB ... MSB-7	R/W
14.	Energy selection upper threshold	ES	16#FF	MSB ... MSB-7	R/W
15.	Delay of CsI detector	CSI_HBR	0	238 nsec – 14.8 µsec	R/W
16.	Delay of CdTe detector	CDTE_HBR	0	238 nsec – 14.8 µsec	R/W
17.	time coincidence acceptance window	TC	0	238 nsec – 61 µsec	R/W
18.	On request value HBR I/F A	HBR_A	16#03	MSByte	R/W
19.	On request value HBR I/F A	HBR_A	16#E7	LSByte	R/W
20.	On request value HBR I/F B	HBR_B	16#02	MSByte	R/W
21.	On request value HBR I/F B	HBR_B	16#00	LSByte	R/W

Table 7: HEPI data register type II (default values shown)

5.2 LUT

The LUT controller accesses to the LUT Ram.
The returned value depends on the calling function.
The rate meters are also integrated within this module.
After power on, the LUT must be filled by DPE with parameters.
The LUT Ratemeters must be set to zero.

The LUT RAM is organized in the following way

5.2.1 LUT organisation

5.2.1.1 Amplitude correction CsI single, multiple

(gain (10 bit) + offset (6 bit)) ∗ 4096 positions = 8192 byte

5.2.1.2 Amplitude correction CsI calibration

(gain (10 bit) + offset (6 bit)) ∗ 4096 positions = 8192 byte

5.2.1.3 Amplitude bin of CsI single histogram

1024 (10 bit) ∗ 1 byte = 1024 byte

5.2.1.4 Amplitude bin of CsI multiple histogram

1024 (10 bit) ∗ 1 byte = 1024 byte

5.2.1.5 Amplitude bin of CsI calibration histogram

1024 (10 bit) ∗ 1 byte = 1024 byte

5.2.1.6 Amplitude bin of CsI polarimetry histogram

1024 (10 bit) ∗ 1 byte = 1024 byte

Total **20k byte**

Start address		Size [byte]
16#0000	Rate meters	8k
16#2000	AC CsI single/multiple event	8k
16#4000	AC CsI cal. event	8k
16#6000	Histogram: CsI single	1k
16#6400	Histogram: CsI mult.	1k
16#6800	Histogram: CsI cal.	1k
16#6C00	Histogram: CsI polarimetry	1k
16#7000	Spare	4k

Figure 5: LUT organisation

5.2.2 LUT Initialisation

After Init command (CID 01) to HEPI the LUT will be initialised as following:

Address $0000 - $1FFF : $00 ...

Address $2000 - $5FFF : $00 $02 $00 $02 ...

Address $6000 - $63FF : $00 $00 $00 $00 $01 $01 $01 $01 $02 $02 $02 $02 ...

Address $6400 - $67FF : $00 $00 $00 $00 $01 $01 $01 $01 $02 $02 $02 $02 ....

Address $6800 - $6BFF : $00 $00 $00 $00 $01 $01 $01 $01 $02 $02 $02 $02 ...

Address $6C00 - $6FFF : $00 $00 $00 $00 $01 $01 $01 $01 $02 $02 $02 $02 ...

The guaranties the unchanged transmission of the CsI events within amplitude correction. The histogram bins are equidistant (4 bins).

6 Mass Memory allocation

The division of the mass memory on HEPI is shown in Figure 6
A linear addressing scheme is used.
A part (8 kbyte) of the LUT-RAM is used for the CsI rate meters.
Access to LUT and mass memory RAM is done by different data and address busses.

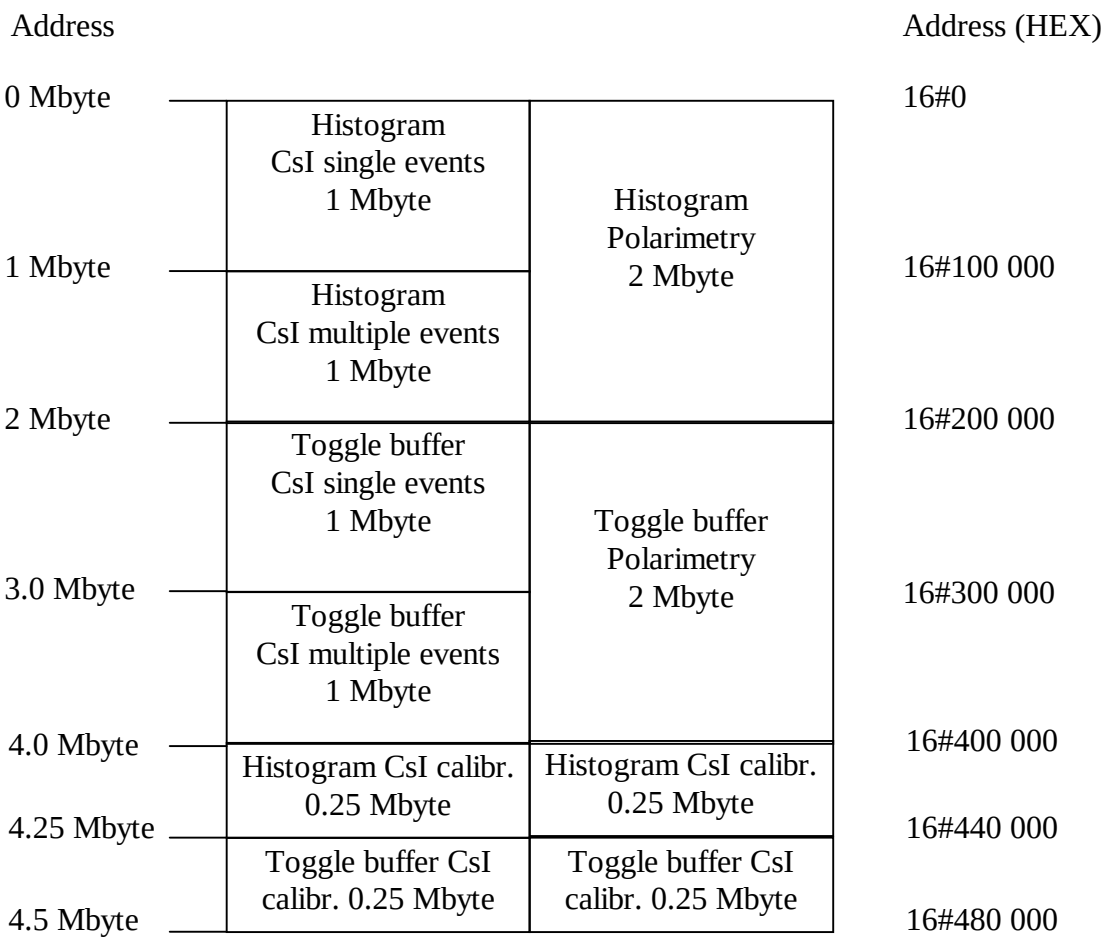

Figure 6: Mass memory organisation

7 Detailed design

In this chapter a description of the detailed design of the different tasks from HEPI is given.

7.1 Overview

An overview of the electronics design of HEPI is shown in Figure 7.
After initialisation of HEPI (via pulse on the reset line from DPE), it will be automatically in a transparent mode. In this mode HEPI reads only in the data from both detectors and then put the data to the HBR I/F A.
In different IASW scientific sub modes are different modules of HEPI active. The modules are selected according Table 4.
The active modules are shown in Figure 8 of transparent mode, in Figure 9 of standard and polarimetry pointing mode and in Figure 10 of PPM and all slew modes.
The larger lines indicates the active paths and the shaded boxes the active modules.

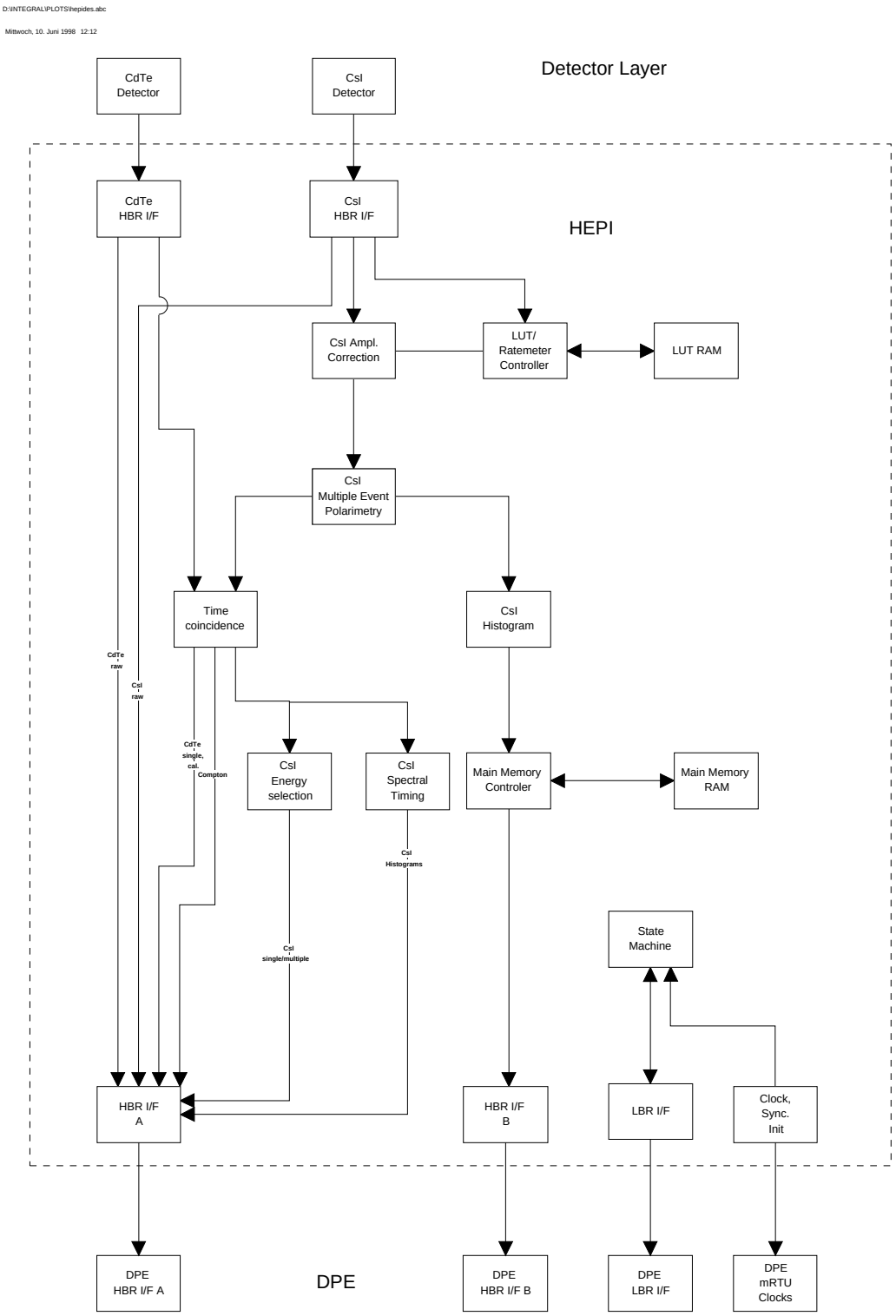

Figure 7: Overview of the HEPI data flow

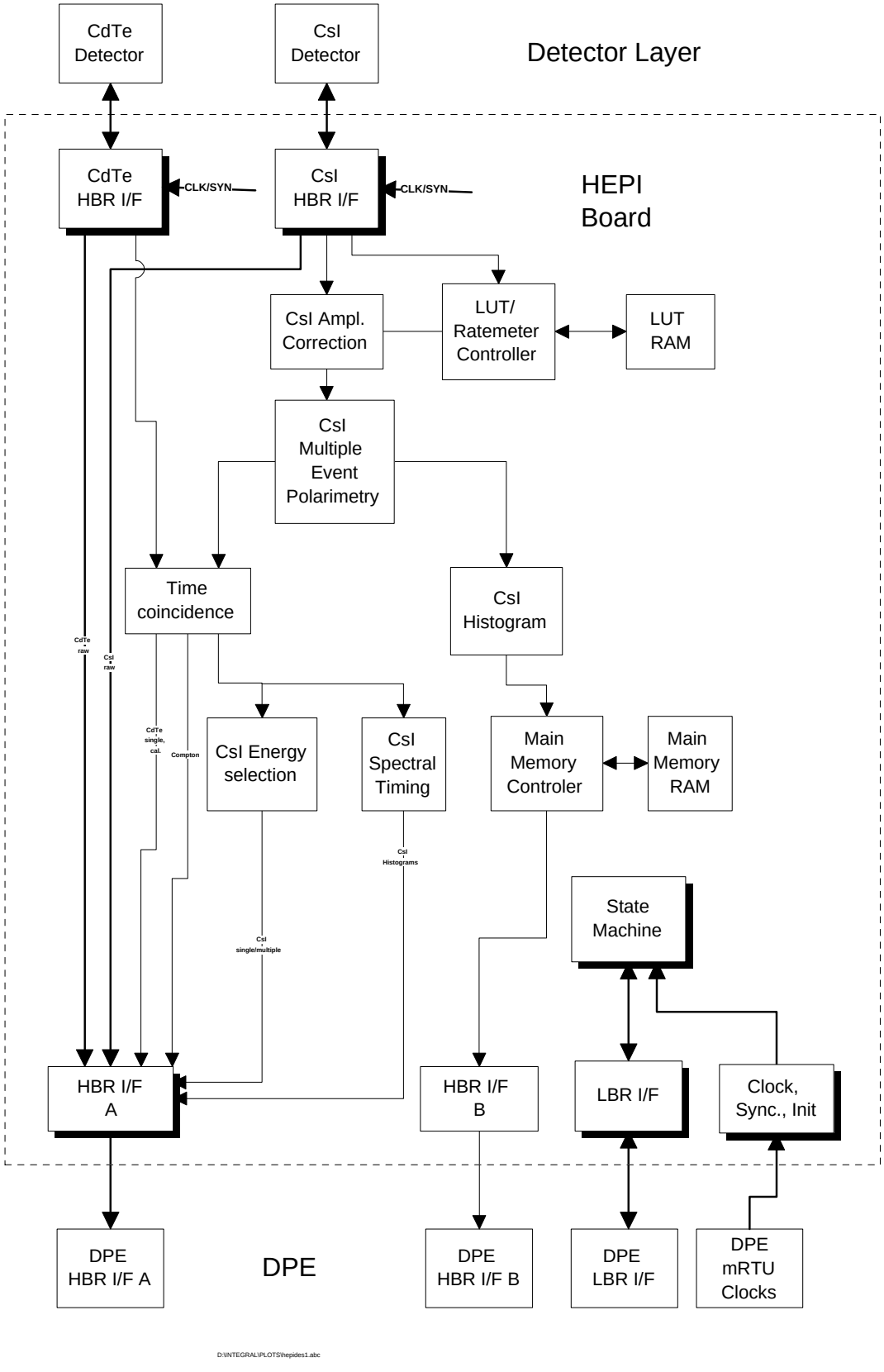

Figure 8: HEPI Data Flow in Transparent Mode

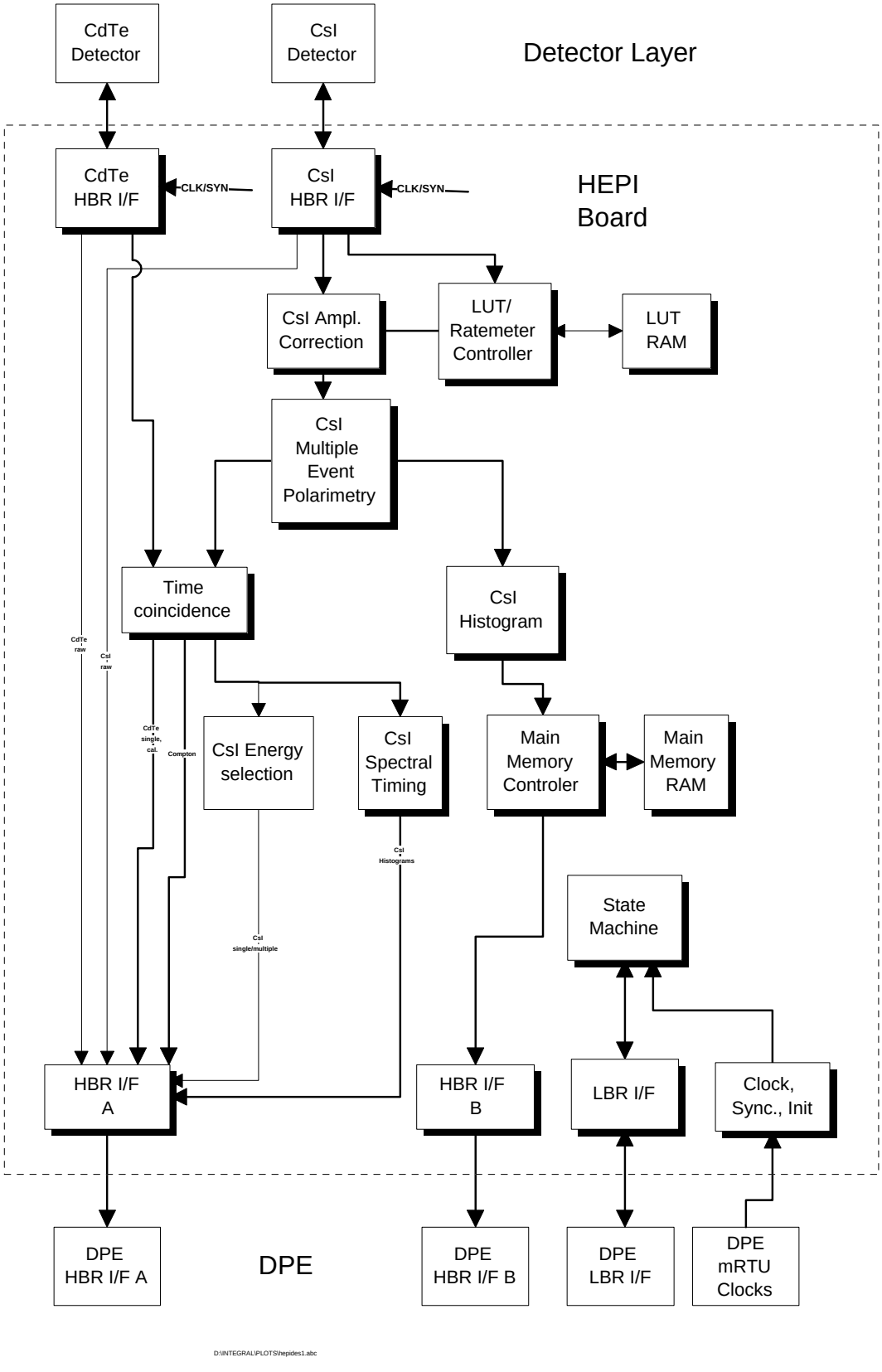

Figure 9: HEPI Data Flow in Standard and Polarimetry Mode

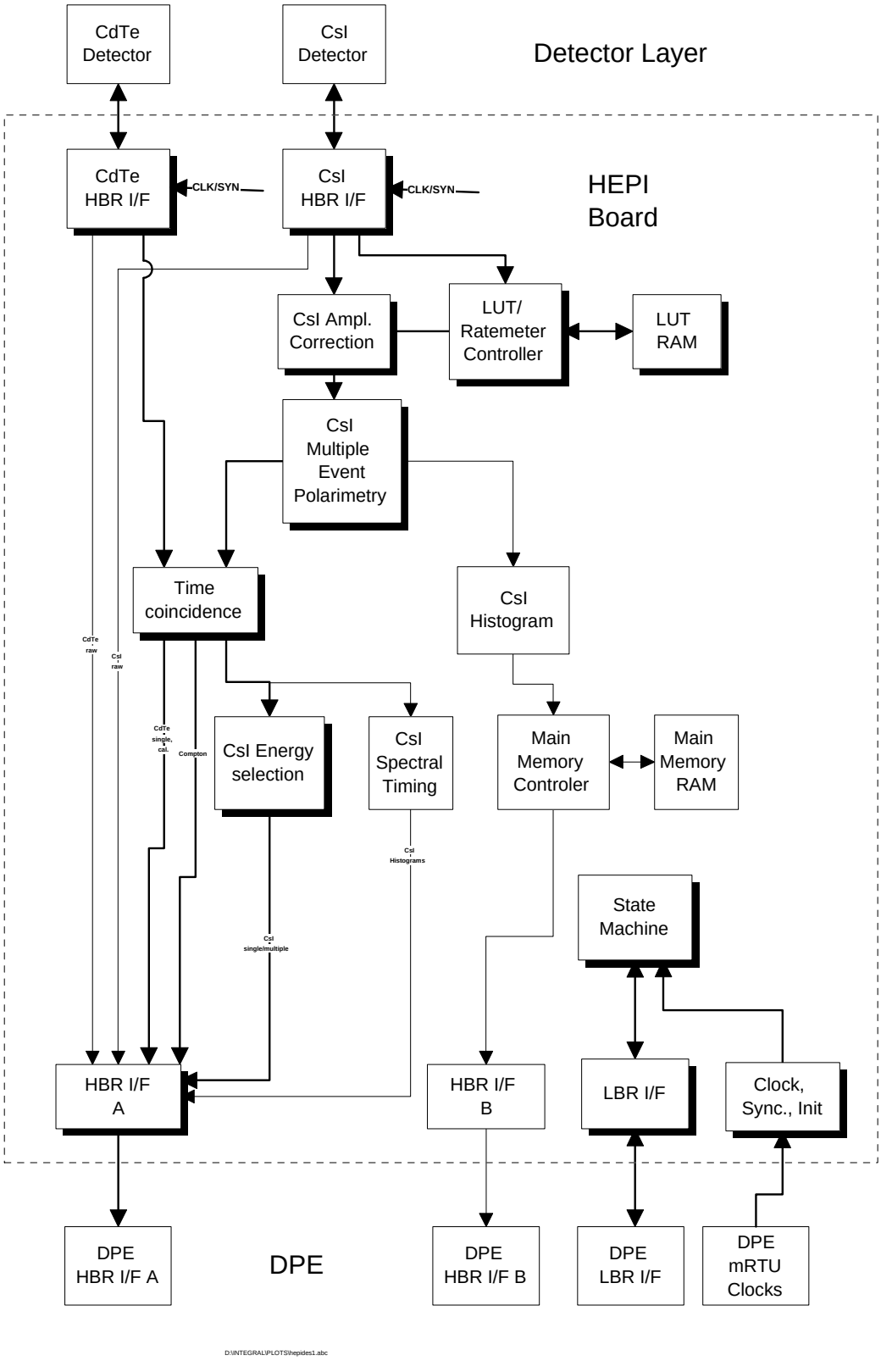

Figure 10: HEPI Data Flow in PPM mode

7.2 Energy correction

The sensitivity of all pixels is not the same. So the delivered amplitude for the same energy is proportional to the energy but different for each pixel. Therefore an amplitude correction (AC) with a linear regression algorithm is needed and shall be applied to each CsI event.

In the transparent status (corresponding control flag in HEPI status register is 0) the amplitude correction module will transmit the data direct without changing them.

For this correction a linear regression algorithm

$A_{out}(i) = a_i + b_i(A_{in}(i))$ i = pixel address

will be used. The precision of the constant a will be 6 bit and of the gain b will be 10 bit. Gain b is a fixed point value with a resolution of 0.002 and a max. value of 1.998 and following bit representation:

Bit	G 0 MSB	G 1	G 2	G 3	G 4	G 5	G 6	G 7	G 8	G 9 LSB
Weight	1	2^-1	2^-2	2^-3	2^-4	2^-5	2^-6	2^-7	2^-8	2^-9

Offset a is a 6 bit value with following bit representation:

Bit	O 0 MSB	O 1	O 2	O 3	O 4	O 5 LSB
Weight	+/-	2^4	2^3	2^2	2^1	1

O 0 is the sign bit: if this bit is set to 1 the value represented by O 1 to O 5 will be subtracted, if bit O 0 is set to 0 the value O 1 to O 5 will be added to the amplitude of the event.

The constants are stored in LUT RAM. CsI single and multiple events are using the same LUT. The LUT of the CsI calibration events is filled with 1 for the gain and 0 for the offset as default values by HEPI. Start address of CsI LUT is 16#2000 for single/multiple and 16#4000 for calibration LUT.

If the result of the amplitude correction is higher than 10 bit range, the result will be become 16#03FF and an overflow flag in the HK will be set. This is also true, if only the result of the multiplication is larger then 16#03FF.

If the result of the offset correction less then 0 it will be set to 0 and an overflow flag in HK will be set.

Data organisation of Amplitude correction LUT in HEPI:

Byte 2n+0

Bit	0 (MSB)	1	2	3	4	5	6	7 (LSB)
	Gain LSB							
	G 2	G 3	G 4	G 5	G 6	G 7	G 8	G 9

Byte 2n+1

Bit	0 (MSB)	1	2	3	4	5	6	7 (LSB)
	MSB Offset LSB						MSB	
	O 0	O 1	O 2	O 3	O 4	O 5	G 0	G 1

With offset (O) and gain (G), amplitude (AM) and corrected amplitude (AC).
AC= AM*G + O

Example: CsI single/multiple amplitude correction with offset 0 and gain=1 (neutral) for pixel address 0 and 1
Address Value
$2000 16#00
$2001 16#02
$2002 16#00
$2003 16#02

or

Byte 2000 or 2002

Bit 0 (MSB)	1	2	3	4	5	6	7 (LSB)
Gain LSB							
0	0	0	0	0	0	0	0

Byte 2001 or 2003

Bit 0 (MSB)	1	2	3	4	5	6	7 (LSB)
MSB Offset LSB						MSB	
0	0	0	0	0	0	1	0

7.3 Multiple event reconstruction

About only 48 % of all photons generate single events in the CsI layer. All other photons generate two (34%) or more (18%) events.

Following reconstruction schemes will be applied to the events:

double:	if ($E_{tot} > E_{thres.}$)	$P_{incident}$ corresponds to max (E_1, E_2)
triple:	if ($E_{tot} \leq E_{thres.1}$)	$P_{incident}$ corresponds to min (E_1, E_2, E_3)
	if ($E_{thres.1} < E_{tot} \leq E_{thres.2}$)	$P_{incident}$ corresponds to mid (E_1, E_2, E_3)
	if ($E_{tot} > E_{thres.2}$)	$P_{incident}$ corresponds to max (E_1, E_2, E_3)

This results in the following energy ranges and resolutions:

	number of bit	energy range	resolution (1 bit)
single:	10	0 - 5 MeV	5 keV
double:			
A(i)[10 bit] + A(i+1) [10 bit] = $A_{mult.}$ [11 bit]	11	0 - 10 MeV	5 keV
cut-off of LSB ⇒	10	0 - 10 MeV	10 keV
triple			
A(i)[10 bit] + A(i+1) [10 bit] + A(i+1) [10 bit] = $A_{mult.}$ [12 bit]	12	0 -15 MeV	5 keV
cut-off of LSB and MSB ⇒	10	0 - 10 MeV	10 keV

Triple events with an energy sum larger as 10 MeV are only counted and then discarded (refer values of CsI events > 10 MeV in HK data).
In the transparent status (corresponding control flag in HEPI status register is 0) the multiple event reconstruction module will transmit the data direct without changing them.

The multiple events will be reconstruct by following scheme:

Preconditions:
- Events generated by same photon are in successive order.
- The multiplicity is the total number of generated events.
- multiple events with calibration flag must be deleted on the detector
- if an overflow/underflow occurs at the previous step (amplitude correction), the reconstructed total energy will not be correct (to less or to high).

MUX: 2#00 single events
MUX: 2#01 double events
MUX: 2#10 triple events

- Events with not valid multiplicities are deleted.
- Multiple module flag and pulse IF is not processed
- Single events are not processed by this module

Events are read in according multiplicity flags (one, two or three events).
Time information is not checked.
The sum of the amplitude is calculated.
The position is estimated according total amplitude and above algorithm.

If the multiplicity of the first event is higher than the number of events with same multiplicity flag, the reconstructed event is deleted.

Is the multiplicity of the first event less then number of events, only the number of events according the first event are processed. The remaining events are processed as an additional event or eventually deleted (depends on the number).

Examples for valid and not valid reconstructed events

Single module

TIME	CAL	MMC	PID	MUX	AMP	POS	
1234	X	0	XX	00	XXXX	XXXX	Single event. no reconstruction required
1234	X	0	XX	01	XXXX	XXXX	1. part of double
1234	X	0	XX	01	XXXX	XXXX	2. part of double
							valid reconstruction
1234	X	0	XX	01	XXXX	XXXX	1. part of double
2345	X	0	XX	01	XXXX	XXXX	2. part of double
							valid reconstruction !!!!
1234	X	0	XX	10	XXXX	XXXX	1. part of triple
1234	X	0	XX	10	XXXX	XXXX	2. part of triple
1234	X	0	XX	10	XXXX	XXXX	3. part of triple
							valid reconstruction !!!!
1234	X	0	XX	10	XXXX	XXXX	1. part of triple
1234	X	0	XX	10	XXXX	XXXX	2. part of triple
1245	X	0	XX	00	XXXX	XXXX	single
							no valid reconstruction because three multiple events are expected. Last single event is only valid event.

Multiple module

TIME	CAL	MMC	PID	MUX	AMP	POS	
1234	X	1	XX	01	XX	XX	1. double, 1. mod.
1234	X	1	XX	01	XX	XX	2. double, 1. mod
1234	X	1	XX	01	XX	XX	1. double, 2. mod

1234	X	1	XX	01	XX	XX	2. double, 2. mod.
							First two events are reconstructed in one valid double event Second two events are also reconstructed in one valid double event.

If one module generate in a time frame one single event and an other module during the same time (time window) a double event, the multiplicity of these three events must set to 3, otherwise the events will not correctly processed.

7.4 Polarimetry of CsI double events

This function computes the scattering angle of CsI double events and accumulates this together with the reconstructed information of position of the incident pixel position and total energy into a histogram. The position of the incident photon is reconstructed as described in section 7.3.

The angles are only determined for events in the direct vicinity of the incident pixel position (see Figure 11).The two data informations of the events are distributed to registers (see Figure 12). The position information is splitted into Y- and Z-values. The Y- and Z-values of the first event are increased by one. After that the values of the second event are subtracted. If the difference is larger then 1, the events are not processed as polarimetry events. This is valid also, if one of the position of the events is near the Y- or Z- boarder, e.g. delta (Y,Z) = pos_1(63,0) - pos_2(0, 63)=(63,-63); the absolute values of both results are larger then 1, so the event is not processed as polarimetry event.

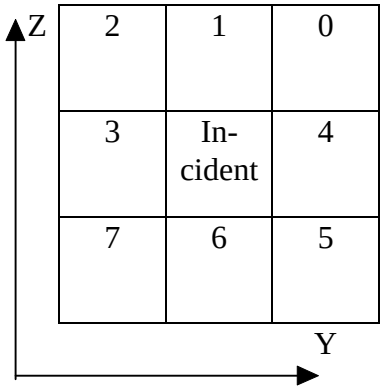

Figure 11: Numbering scheme of scattered photons

From the previous calculation we get two 2 bit values of the differences. Only eight values are possible because the differences are lower or equal three and the sum of the differences is greater zero. This three bit information and a six bit energy value are stored in a histogram similar the CsI single and multiple event histograms. This is not shown in the sketch.

The polarimetry function is implemented in the multiple event reconstruction module.

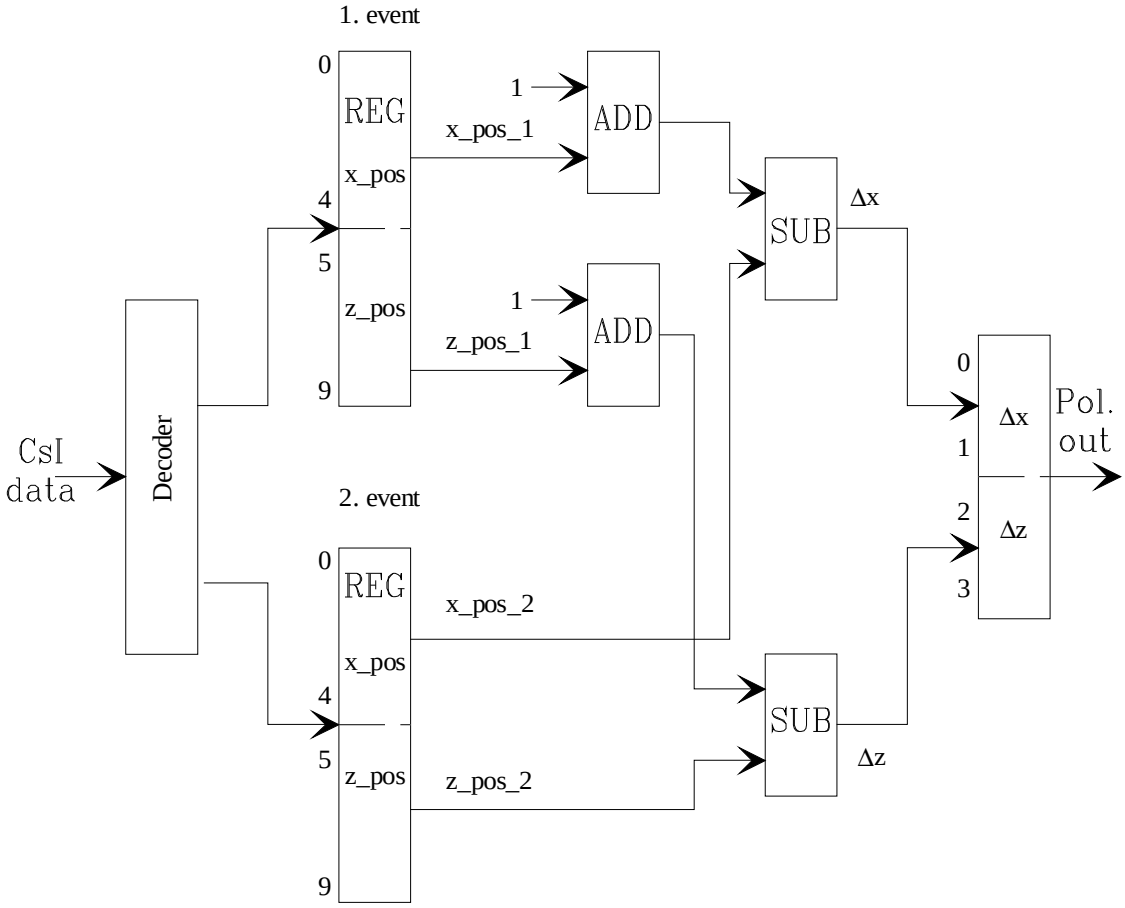

Figure 12: Principle of polarimetry process

(Y/Z)	POL(2:0)	Decimal code
(0/0)	000	0
(1/0)	001	1
(2/0)	010	2
(2/1)	011	3
(0/1)	100	4
(0/2)	101	5
(1/2)	110	6
(2/2)	111	7

Table 8: Coding scheme for CsI polarimetry events

Table 8 shows the coding scheme of the 8 different positions (Y/Z).

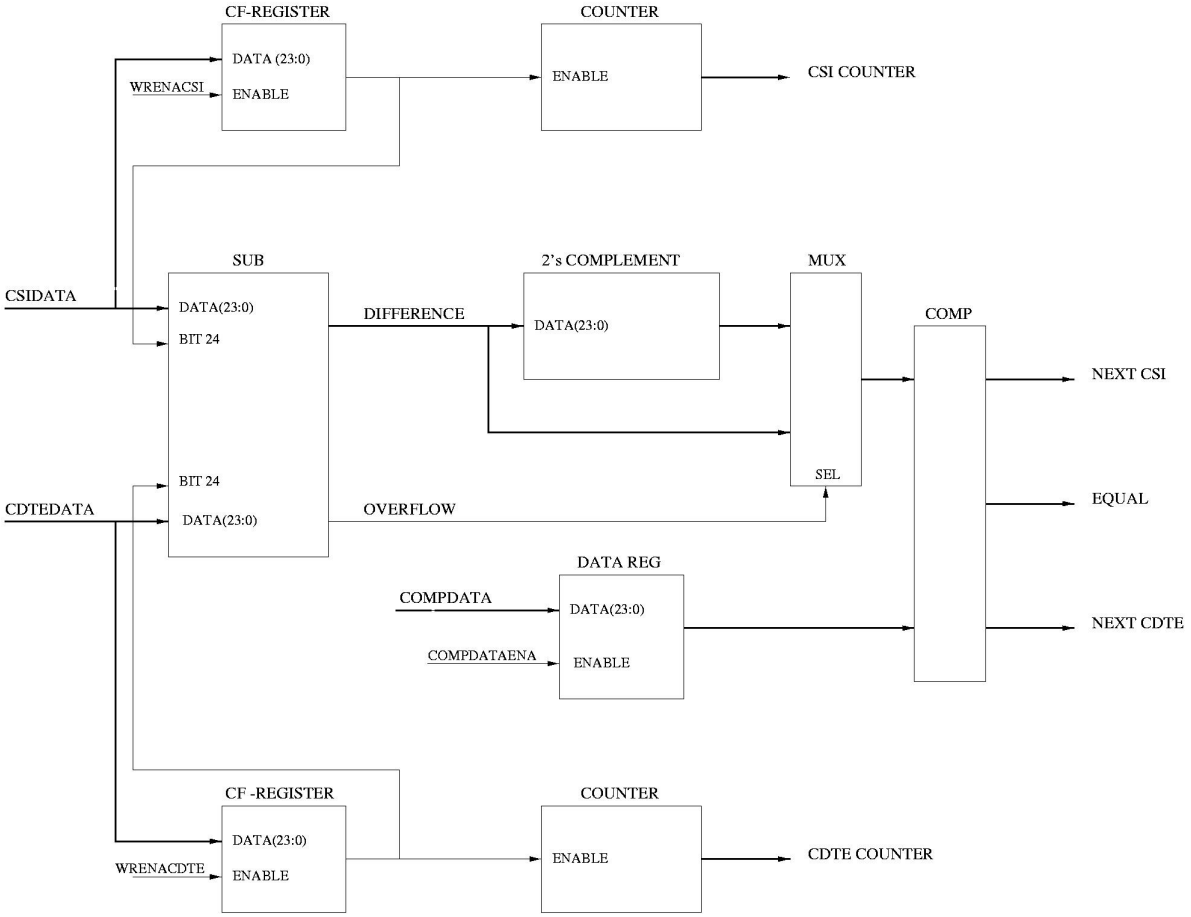

Figure 13: Detection of time coincidence between CsI and CdTe events

7.5 Time coincidence of CsI and CdTe events

The detection of time coincidences is based on a comparison of the two timing informations. If the difference is lower or equal than a programmable time window width the events are thought to originate from the same incident photon.
Timing information is generated within the detectors by counting the 4Mhz clock. Each 2 sec this counter is cleared from the sync-pulse generated by HEPI. So normally a 23 bit information is generated. In case of malfunction of the clock or sync the 24th bit is although set (more than 2^23 clocks between two sync-pulses). Events with 24th bit set will be deleted on this module.
The detection of time coincidence could be switched off by setting the corresponding control flag in HEPI status register.

For detecting time coincidences first the CsI and CdTe time information (23 bit) are subtracted (sub) to get the difference of the two values (see Figure 13). If the CdTe time is greater than the CsI an overflow occurs. In that case the 2's complement of the difference is created to get the correct value. This value is compared with the range value in the data register (time window). Both times are equal, if the difference of CsI and CdTe time data is equal or lower than the

range value. If the difference of CsI and CdTe is greater than the range value the next CdTe event is read, or the next CsI in case of an overflow.
To get an information if a zero crossing (reset of the time counters of the detectors) has occurred in the data stream of the time information, the carry flag register and the 24th bit is set if the previous event time is greater than the next event time. If an overflow at the other event type occurs the flag will be reset.
Simultaneously the counter is increased by one and can be read out for control purposes and to get the synchronised timing information until start of the observation.
Each incoming event is counted and the value of this counter could be read out with a dedicated command.
The timing information of each event is reduced to 15 bit (time resolution of 64 μsec) and than increased by the content of the zero crossing counter (17 bit). This leads to a time resolution of 64 μsec within 72 h.
Pre-conditions:

- Events must be time sorted
- Events should not have time information larger 23 bit representation (24 bit representations are deleted in this module)
- more than one event each 2 sec event rate of each detector.
- if only one detector is connected, either the other detector I/F must be switched off or the time coincidence detection. This could be done setting the correct control bits in HEPI control register. Otherwise data processing will be stopped in HEPI.
- If both calibration flags of the events are set, a different compton type (compton calibration, B4) will be generated. If only one of both events calibration tagged, then the corresponding bit in the data field will be set and the event is combined as a standard compton event (A4).

7.6 Accumulation of CsI events

The CsI single, multiple, calibration and polarimetry events are accumulated in a SRAM (histogram mode) without time information. The position, the event type and a look up table of the energy select the cell of the RAM which is increased by one.
The look up table contain 8 bit values of the energy channels.
The energy values (10 bit width) of the CsI events are binned into energy channels using the look up table. The memory area bits, channel number, type and position of the event select the cell of the RAM, which is increased by one. If the value exceeded 255 a dedicated overflow flag in the HK data is set and the value will be hold on 255.
After integration the RAM can be read out.
To avoid that during read out the scientific data lost, a second memory area is used to collect the data of the next integration cycle. Switching between these areas is done via command of the IASW (change of the memory area bits). Calibration and science histograms use independently memory areas.
The start and stop of the integration is controlled by DPE commands. An additional command could clear parts of the memory area.
Following memory mapping was chosen:
HEPI Histogram Memory Mapping

Histogram Type	Start Address	Stop Address
Polarimetry (0)	$000 000	$1FF FFF
Polarimetry (1)	$200 000	$3FF FFF
Single (0)	$000 000	$0FF FFF
Single (1)	$200 000	$2FF FFF
Multiple (0)	$100 000	$1FF FFF
Multiple (1)	$300 000	$3FF FFF
Calibration (0)	$400 000	$43F FFF
Calibration (1)	$440 000	$47F FFF

(0)/(1): Memory area I / II

The 23 bit memory address is composed as following:

Polarimetry: 0SYYYYYYZZZZZZPPPBBBBBB

Calibration: 1000CYYYYYYZZZZZZBBBBBB

Multiple: 0S1YYYYYYZZZZZZBBBBBBBB

Single: 0S0YYYYYYZZZZZZBBBBBBBB

Where

S = Memory Area I or II
C = CAL Memory Area I or II
Z = CSI Z-POS(5:0)
Y = CSI Y-POS(5:0)
P = Polarimetry Angle (2:0)
B = Energy (7:0)

This quite complicate scheme was chosen, because in case of lost of one TM packet, you loose only the information of one pixel. This is more easy to reconstruct than the lost energy band for a lot of pixel. This scheme was also proposed by ISDC and ESA.

7.7 Spectral timing

This module accumulates CsI single and multiple events in histograms with 8 energy channels within a variable short time period. The time period will be programmable from 0.976 msec up to 500 msec.
Following representation of the integration time value is valid :
Integration time is 2^(-10 + value in register)

Register	0	1	2	3	4	5	6	7	8	9

value										
Integration time [msec]	0.97	1.95	3.91	7.81	15.6	31.3	62.5	125	250	500

The value of the events energy is binned into 8 channels with nine comparators and the corresponding counter is increased by one. The counters are read out when the time difference between the next event and the starting time of integration is greater than a programmable threshold. Then the register are cleared and a new integration cycle starts. The start time of the new integration is the start time of the previous one plus integration time. The first integration time is the time of the first event after switching on the spectral timing.

Following representation of energy thresholds is valid:
All nine thresholds are stored in 8 bit registers. The resolution of the lowest bit is 2^3*(resolution of LSB of CsI events). The resolution of the CsI events is about 5 keV. This leads to an energy resolution of the thresholds of 40keV. The maximum threshold (16#FFFF) is then 10.2 MeV.
A counter (n) is selected according a lower threshold (n) and a higher threshold (n+1).The counter value increases by one if the amplitude value of the CsI event is higher equal than the lower threshold and lower than the upper threshold.
The position information of each event is discarded.
The start of integration time is included within the packet.
If there is no event within the counters during one integration interval, the outgoing packet is not generated.

Constraints:

- events must be ordered by time
- time difference between two successive events must be less equal 32*integration time (e.g. a integration time of 0.97 msec leads to a maximum time gap of 31.25 msec between two successive events)

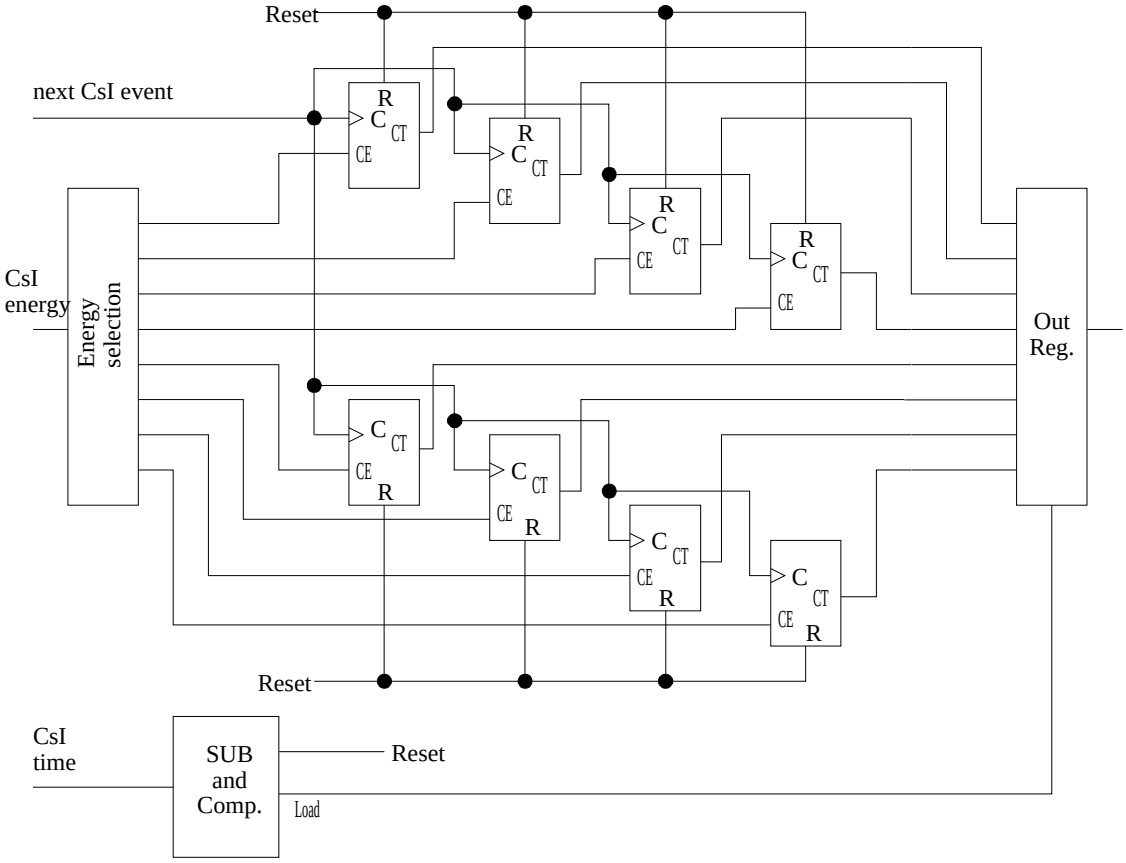

Figure 14: Principle of spectral timing

7.8 Energy selection

For the Photon by Photon mode of the CsI events a energy selection is applied. A lower and upper threshold (8 bit) is applicable to the corrected amplitude values of CsI events.
The resolution of the lowest bit is 2^3*(resolution of LSB of CsI events). The resolution of the CsI events is about 5 keV. This leads to an energy resolution of the thresholds of 40keV. The maximum threshold (16#FFFF) is then 10.200 MeV.
The events are transmitted, when the amplitude is higher equal than the lower threshold and lower equal than the upper threshold. The selection reduces the expected data rate and the DPE can continue the data processing of this events after handling over the HBR I/F A.

7.9 Rate meters

For the CsI events individual counters are applied to each pixel position. The width of the counters is 16 bit. The ratemeters share the memory with the LUT of the HEPI.
Start, stop and clear is controlled by dedicated TC.
In case of overflow of one rate meter the counter will be set to 16#FFFF and a dedicated flag will be set in HEPI HK.

7.10 Delay of synchronisation pulse of detectors

HEPI distributes a individually delayed synchronisation pulse to each detector. The delay time is adjustable from 238 nsec – 15 µsec.

7.11 Heart Beat

To control, if HEPI gets the 4 MHz and BCP2 from DPE, a function is implemented, which generates a 0.5 Hz signal. If this signal is on, both 4 MHz and BCP2 are available from DPE. This signal could be sampled by the DPE on the status line.

8 Electronic layout

Figure 15 show a preliminary layout of the two PCB's. The main data streams are grey shaded.
The two boards are connected with an internal connector.
The FPGA or ASIC is placed on the main board (left side of Figure 15).
The front connectors are also connected to the main board.
The memory (right side of Figure 15).board contains only parts of the memory (3 Mbyte).

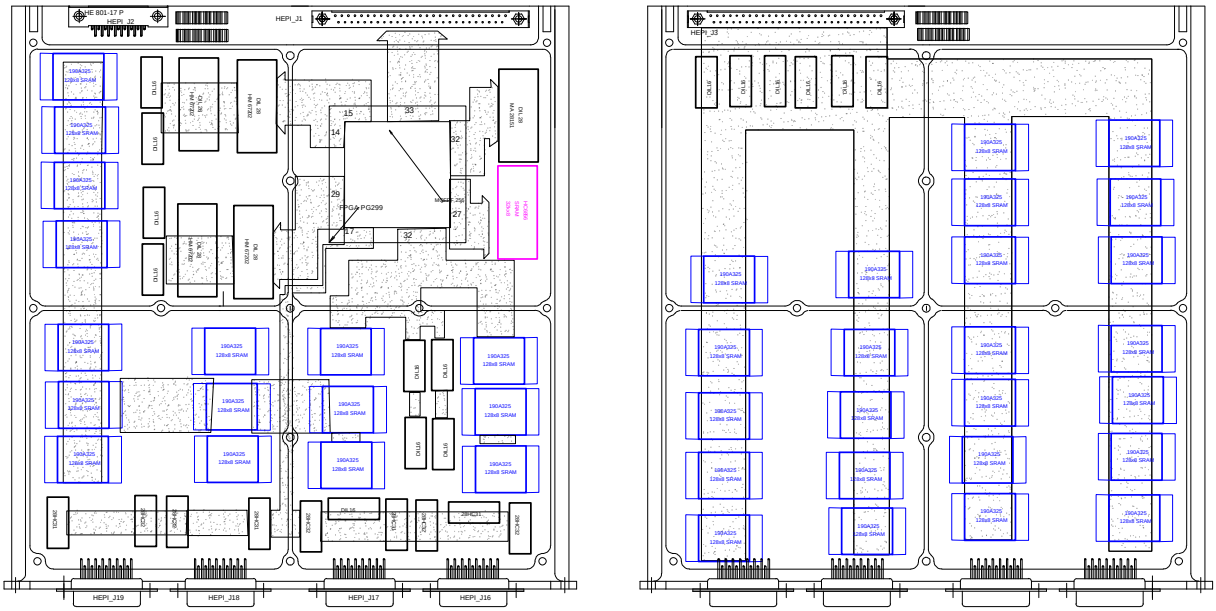

Figure 15: Preliminary layout of the electronics

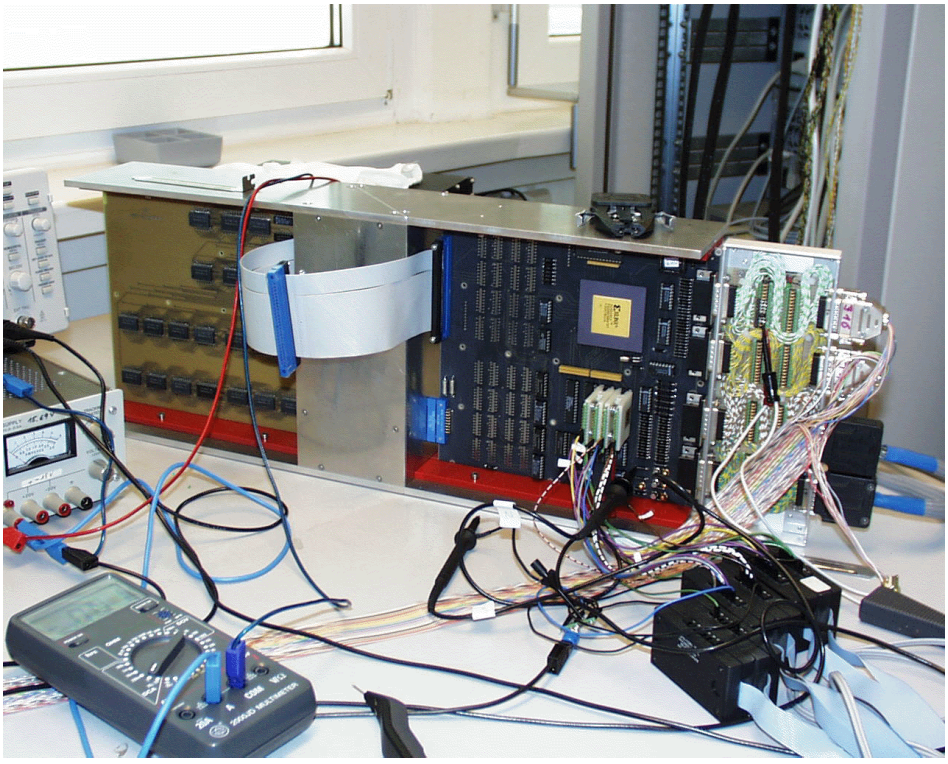

Figure 16: HEPI test environment

Figure 16 shows the HEPI test environment. On the left side the memory card is shown, the right side shows the HEPI main board with FPGA. For better testing both cards are hold by a test frame.
After integration both cards are mounted in frame (Figure 17), which is plugged directly into the DPE.

Figure 17: HEPI mounting frame