Title: **HEPI Interface Description**

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	5.5	3.2., 3.3	Power allocation, power distribution
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1 References

1.1 Applicable documents

AD.1: EID-A rev. 4
AD.2: INT-DD-CRS 001, DPE HW design description

1.2 Reference documents

RD 1: HEPI Design Description, IN-IM-TUB-DES-001, IS. 5
RD 2: IBIS Communication Protocol Definition, IN-IM-TUB-ICD-01, Is. 1

2 Electrical Interfaces of HEPI

2.1 General

For controlling and HK the detectors, veto and HEPI are connected via slow serial bus interfaces to DPE . The receiver will be selected by individual lines.

The data are linked from each detector (ISGRI and PICSIT) through a High Bit Rate Interfaces to HEPI. After pre-processing the HEPI sends the data through two HBR I/F to DPE.
A status line from HEPI to DPE controls the HEPI status (test I/F).
A ON/OFF line controls the HEPI initialisation.

2.2 Overview of the interfaces

2.2.1 DPE – HEPI

- Low Bit Rate Interface (LBR I/F)
  -3 serial lines
- On Board Clock Bus (2 lines)
  - general clock line
  - general synchronisation line
- Fast serial line interfaces A and B (each 4 lines)
  -data (from HEPI)
  -enable (from DPE)
  -request (from HEPI to mRTU)
  -clock (from DPE)
- status line from HEPI to DPE (one line)
- Init HEPI line (from DPE to HEPI) (one line, Pulse 7)

2.2.2 HEPI – CdTe detector

- Fast serial line interface (6 lines)
  -data (from detector)
  -sample (from HEPI)
  -FIFO not empty (from detector)
  -clock (from HEPI)
- delayed synchronisation for CdTe detector (from HEPI)
- Clear_FIFO line (from HEPI)

2.2.3 HEPI – CsI detector

- Fast serial line interface (6 lines)
  -data (from detectors)
  -sample (from HEPI)
  -FIFO not empty (from detector)
  -clock (from HEPI)
- delayed synchronisation for CsI detector (from HEPI)
- Clear_FIFO line (from HEPI)

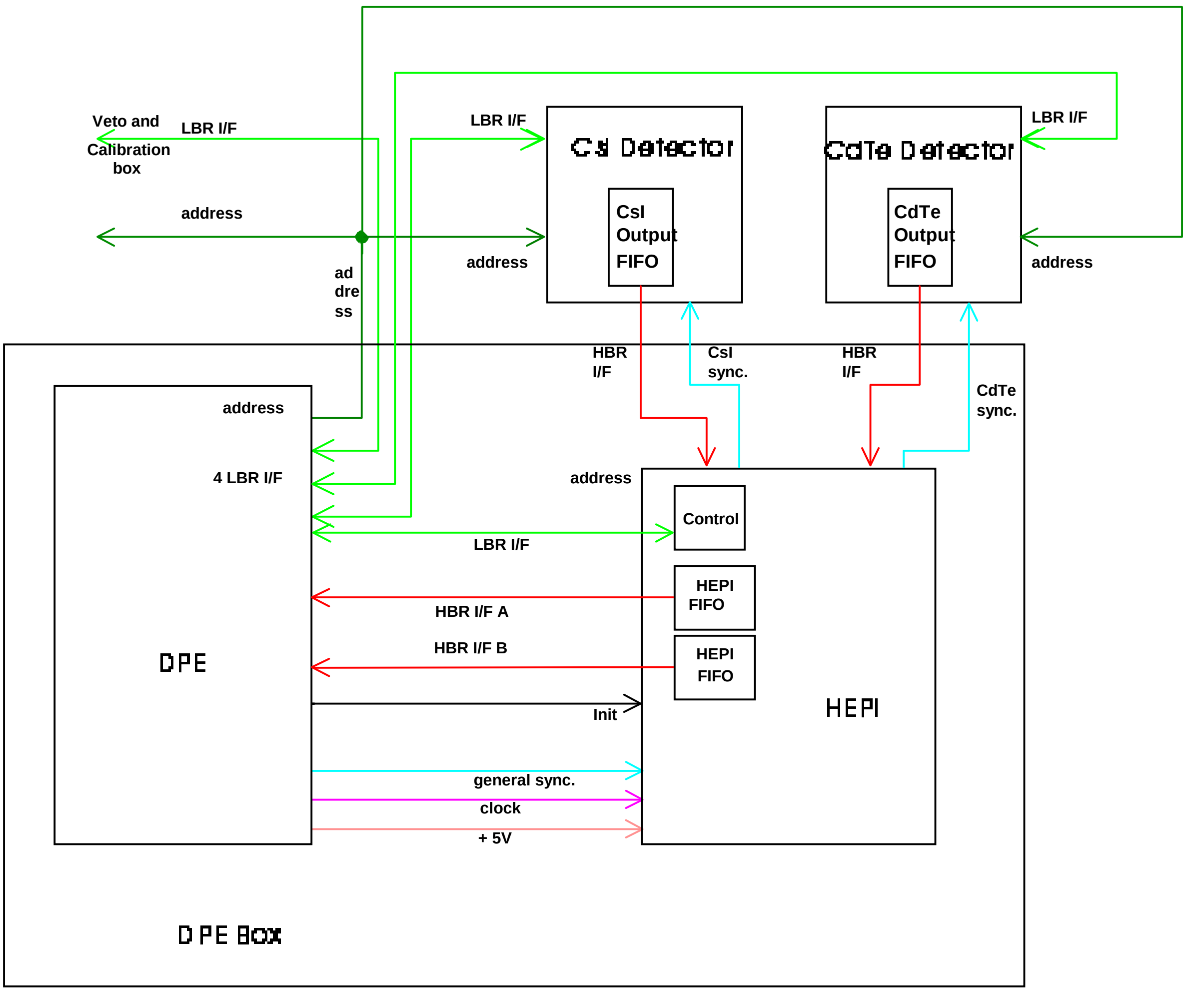

Figure 1: Overview of the electrical interfaces of the HEPI

2.2.4 Distribution of timing and synchronisation information

For timing and synchronisation purposes the DPE generates and distributes a 4,194,304 Hz clock and a 1 sec pulse (BCP 2) with 1.9 µsec pulse width..

From the 1 sec pulses HEPI generates synchronisation pulses with a 2 sec time period. The timing is shown in Figure 2. The sync-line goes low with the rising edge of the clock (plus internal propagation delays). The pulse width of the HEPI generated sync pulse is one clock cycle (238 nsec).

To compensate the delay of each detector electronics this pulse is individually delayed and distributed to ISGRI and PICSIT and resets every 2 sec the detector time counters.

2.2.5 Starting and timing of an observation cycle

The DPE initialises the observation at the time t_{n-1} with a dedicated telecommand. At t_n (cf. Figure 2) HEPI generates a new synchronisation pulse and with the rising edge of the clock pulse HEPI clears the output FIFOs. The clear FIFO lines from HEPI to the detectors goes low. The pulse width of the FIFO reset pulse is also on DPE clock cycle (234 nsec).

The time difference between t_n and t_{n-1} is 1 sec.
The detectors fill their output FIFOs with newly measured events and mark them with a time tag with 238 nsec time resolution within 2 sec (23 bit). HEPI reads them out and looks for time coincidences between the two detector layers.
Then the last 8 bit of the time information are cut off and 17 bit additional time information is added to the time field. The resulting time resolution is 61.035 µsec within 72.8 h (32 bit).
With this time information the events are handed over to the DPE. The DPE calculates from this information the time of the events in spacecraft time units and puts them into the data packages.

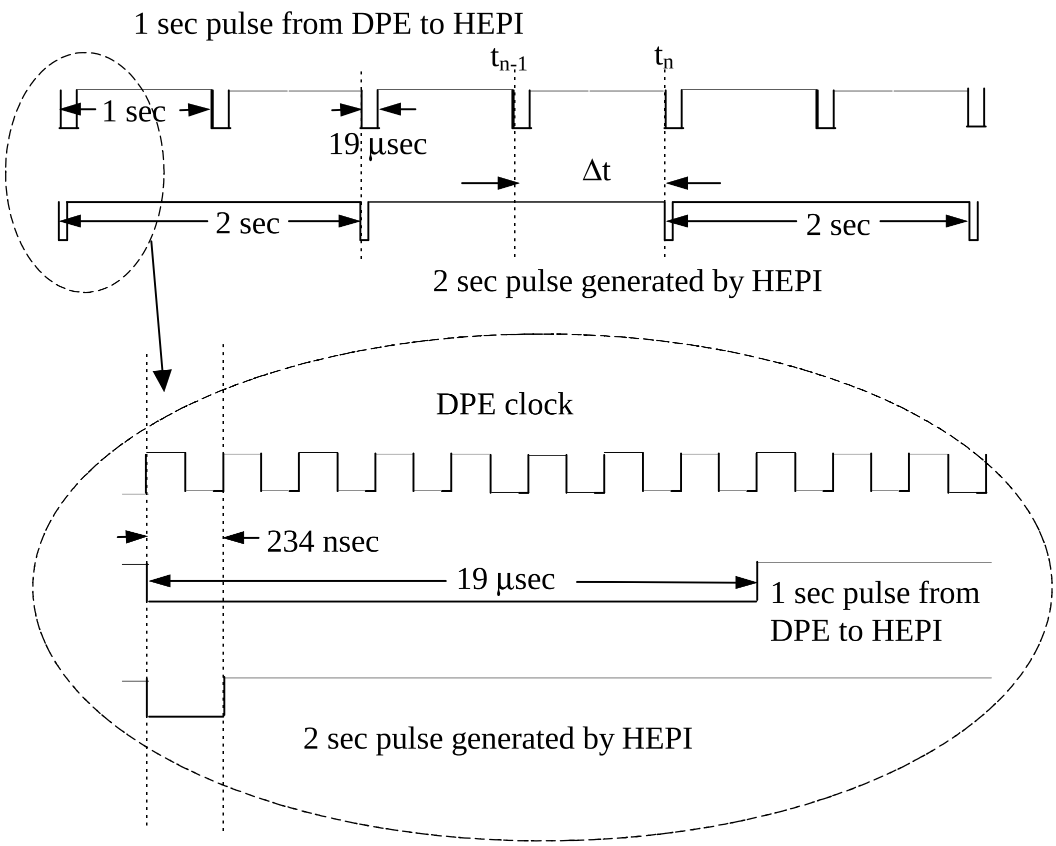

Figure 2: Timing and synchronisation scheme from HEPI and DPE

2.3 Data rates

2.3.1 HBR I/Fs detectors to HEPI:

max. theor. data transmission of each I/F 65,536 events/sec ∗ 64 bit event

4,194,304 bit/sec

expected data rate from ISGRI [1]	1220 events/sec ∗ 64 bit/event	
		78,080 bit/sec
expected data rate from PICSIT	2,000 to 25,000 events/sec∗64 bit/event	
		1,600,000 bit/sec
Total input to HEPI		**1,656,960 bit/sec**

2.3.2 HBR I/Fs HEPI to DPE

max. theor. data transmission	5,000,000 bit/sec	
expected data rate HBR I/F A:		
CdTe Photon by photon	980 events/sec ∗ 80 bit/event	
		78,400 bit/sec
Compton	240 events/sec ∗ 160 bit/event	
		38,400 bit/sec
CsI photon by photon (spectral timing, 1ms)	1,024 events/sec ∗ 160 bit/event	
		163,840 bit/sec
	total A	**280,640 bit/sec**
expected data rate HBR I/F B:		
histograms	2,359,296 byte	
8 byte header / 1992 byte	9475 byte	
transmission time 1300 sec		
	total B	**14,577 bit/sec**
Total expected data rate between HEPI and DPE		**295,217 bit/sec**

2.4 Interfaces DPE – HEPI

2.4.1 Low bit rate interface

2.4.1.1 Timing of LBR I/F

This I/F has following the functions on HEPI:

- receiving control commands for different processing tasks from DPE
- loading look up tables (LUT) and registers (thresholds etc.) with values from the DPE
- controlling the status of the HEPI (HEPI will send HK data and the content of LUTs and registers on request from the DPE)

The Low Bit Rate Interface (LBR I/F) of the DPE consists of the
Slow Serial Lines:

-clock (from DPE),
-forward data (from DPE),
-return data (to DPE);

[1] potential higher during on ground calibration

The data link between the units is bi-directional and under control of the DPE. For communication a asynchronous data link control protocol is applied.
Following protocol is used:

1 start bit,
8 data bit,
1 even parity bit,
1 stop bit.
baud rate factor 1x (16 kHz clock frequency will be delivered by the DPE)

The maximum transmission rate in the asynchronous mode is 16k baud.
For using one start, eight data, one parity and one stop bit the effective rate is about 9800 bit/sec.
The clock line is still used but the DPE programmed frequency is reduced to 16 384 Hz.
The selecting of the HEPI is done by enable one of the four LSL lines.
Then DPE sends commands to HEPI with or without parameters. Receiving of data are detected by the start bit of the transmitted data word (line goes to zero). This line is sampled again at the centre of the expected width of the start bit. If this data is also low, the next data are assumed as valid. Each data will be sampled at the centre.
The LSB of the data word will be received or transmitted first!.
Depending on the command HEPI sends back data and DPE is waiting a TBD time for input.
After end of data DPE unselect the LSL line and the communication is finished.
The functionality of the asynchronous protocol is implemented inside the FPGA/ASIC.
Figure 3 shows the timing scheme of the LBR I/F.

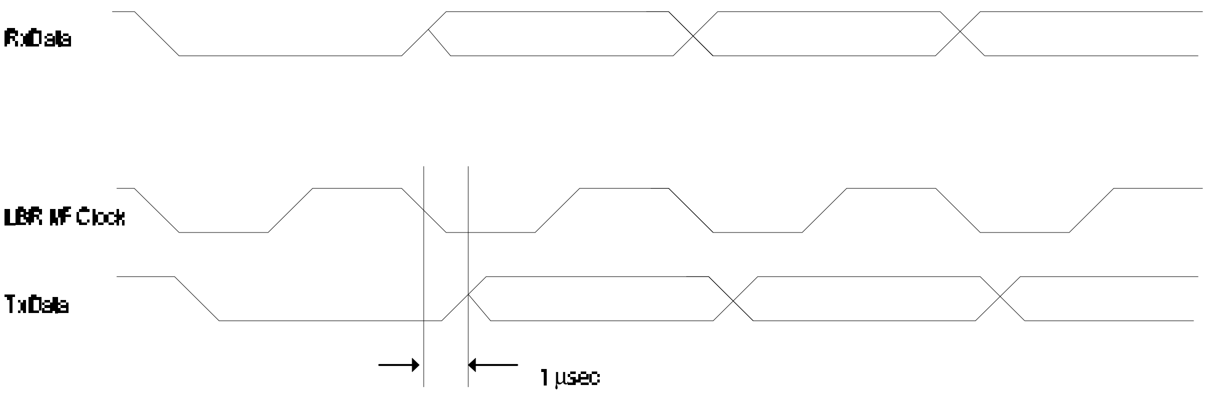

Figure 3: Timing scheme of LBR I/F

2.4.1.2 HEPI control command

All internal data exchanges between DPE and HEPI should have even numbers of bytes.
The first transmitted byte of a data block contains the length of the block in 16-bit words.
Figure 4 shows the general command format on the LBR I/F.

Byte	#1	#2	#3	#4	#5	#6	#7 .. n

Word	#1		#2		#3		#4 ... N
Commands without parameter	Length	Command ID	APID	SUB ID	PSC (MSByte)	PSC (LSByte)	
Commands with parameter	Length	Command ID	APID	SUB ID	PSC	PSC	parameter field

Figure 4: LSL command structure

Word #1/Byte #1: block length (range: 1..120 word (16 bit)) of the complete command block

Word #1/Byte #2: command ID of the peripheral command. The operator code should not exceed 1 byte.

Word #2/Byte #3: APID: The APID (bit 3 to bit 10) of the IASW (nominal or redundant) which is sending the command.

Word #2/Byte #4: SUB ID: The Instrument Sub Address of the receiver (HEPI=0).

Word #3/Byte #5..6: Packet Sequence Control (PSC).

Bit 0 ..1: set to "11"

Bit 2: 0 for commands from ground
1 for on board commands

Bit 3 ..15: Sequence counter of commands related to APID (for on ground generated commands) and sub instrument address (only for on ground generated commands).

Word #4 ..N: parameter field if required. The parameter field should have an even number of bytes.

Table 1 lists the available HEPI control commands. Each command starts with the length field (LGTH) and the command ID number (CID). The expression " _(number of required bytes)" is appended to each parameter, i.e. status_3 requires three bytes for HEPI status word.

C_ID	Acronym	Format	Command Description	Size [word]
C1.001	H_HEPI_INIT	LGTH,CID, APID,SUB-ID,PSC	Init HEPI: Clears all HEPI Register Clears Main Memory Clears Csl rate meter Clears HEPI HBR I/F FIFO Clears Detector FIFOs HEPI goes in transparent mode Set default values for internal type II register.	3
C1.002	H_HEPI_RES	LGTH,CID, APID,SUB-ID,PSC	Clears HEPI HBR I/F FIFO Clears Detector FIFOs HEPI goes in transparent mode Set default values for internal type II register.	3
C1.003	H_S_HEPI_ST	LGTH,CID, APID,SUB-ID,PSC,status_3,00	set the HEPI status register	5
C1.004	H_HEPI_ST	LGTH,CID, APID,SUB-ID,PSC	Read the HEPI status register	3
C1.009	H_S_LUT_RAM	LGTH,CID, APID,SUB-	Set LUT RAM via LBR I/F	69

		ID,PSC,start_2,data_128		
C1.010	H_R_LUT_RAM_LBR	LGTH,CID, APID,SUB-ID,PSC,start_2	Read LUT RAM via LBR I/F from start to start+128-1	4
C1.012	H_R_MEM	LGTH,CID, APID,SUB-ID,PSC,start_2	Read the contents of the memory from start_2*1024 to start_2*1024+1023	4
C1.013	H_CLR	LGTH,CID, APID,SUB-ID,PSC,Mask_2	Clear Counter and Register within HEPI (ref. Table 2)	4
C1.079	H_STR_SYNC	LGTH,CID, APID,SUB-ID,PSC	Start synchronisation with next synch. Pulse	3
C1.117	H_RD_REG_II	LGTH,CID, APID,SUB-ID,PSC	Read register type II (ref. Table 5)	3
C1.118	H_RD_HK	LGTH,CID, APID,SUB-ID,PSC	Read standard HK	3
C1.121	H_S_REG	LGTH,CID, APID,SUB-ID,PSC,register_22	Set register type II	14
C1.122	H_CLR_RM	LGTH,CID, APID,SUB-ID,PSC	Clear ratemeters	3
C1.124	H_CLR_MEM	LGTH,CID, APID,SUB-ID,PSC,start_3,Stop_3	Clear Memory from start to stop address	6

Table 1: HEPI control commands

Bit-Mask	Description
0	clear out - FIFO of the CdTe detector
1	clear out - FIFO of the CsI detector
2	clear out FIFO A of HEPI
3	clear out FIFO B of HEPI
4	Clear the counter of CsI events
5	Clear CdTe event counter
6	Clear the counter of the > 10MeV mult. events
7	Clear zerocrossing counters CdTe,CsI
8	Clear counter executed commands
9	Clear counter requested commands
10	Clear Counter rejected commands
11	Rate meters
12	Amplitude Correction
13	Spectral Timing
14	Memory
15	Spare

Table 2: Bit Mask of Clear_CT_REG command (C1.013)

2.4.1.3 HEPI data block format of LBR I/F

Table 3 shows the HEPI data block format for transmission between HEPI and DPE via LBR I/F. Each data block is transmitted only on request with a dedicated request command by DPE. The first byte of the data blocks contains the length in 16 bit words and the second byte the data block type. This type is identical to the number of the request command.
The values in brackets are showing the position of each data.

	Length (word)	Type			
(Byte No.)	3 (0)	4 (1)	HEPI status register (2..4)		Spare (5)
	66	10	Start	LUT RAM dump	

{Byte No.}	{0}	{1}	{2..3}	{4...131}
{Byte No.}	2 {0}	111 {1}	Register number {2}	Value {3}
{Byte No.}	12 {0}	117 {1}	Data Type II data {2 ..23}	
{Byte No.}	42 {0}	118 {1}	HEPI HK data field {2..31}	On event message field {32..83}

Table 3: On request data format between HEPI and DPE

The HEPI HK data are listed in Table 4 and Table 5. The essential HK data will be send each 8 sec after a dedicated command from DPE to HEPI. The on request HK data type I are thresholds and register values and type II are memory dumps of the LUT of HEPI. They will be send on request after with a dedicated command from DPE.
The command protocol is according RD2.

Register number	Description	
1.	HEPI Status	MSByte
2.	HEPI Status	2nd byte
3.	HEPI Status	LSByte
4.	Counter CsI events	MSByte
5.	Counter CsI events	3rd byte
6.	Counter CsI events	2nd byte
7.	Counter CsI events	LSByte
8.	Counter CdTe events	MSByte
9.	Counter CdTe events	3rd byte
10.	Counter CdTe events	2nd byte
11.	Counter CdTe events	LSByte
12.	number of CsI events > 10 MeV	MSByte
13.	number of CsI events > 10 MeV	LSByte
14.	Zerocrossing counter CdTe events	MSBit
15.	Zerocrossing counter CdTe events	Bit 15 .. 8
16.	Zerocrossing counter CdTe events	LSByte (Bit 7..0)
17.	Zerocrossing counter CsI events	MSB
18.	Zerocrossing counter CsI events	Bit 15 .. 8
19.	Zerocrossing counter CsI events	LSByte (Bit 7..0)
20.	Number of received commands	
21.	Number of request	
22.	Number of rejected commands	
23.	Last command	
24.	Error Register I	

Register number	Description	
25.	Spare	
26.	Spare	
27.	Spare	
28.	Spare	
29.	Spare	
30.	Spare	
31.	Spare	
32.	Spare	
33.	Valid on event messages	MSByte
34.	Valid on event messages	LSByte
35.	Message #1 Sub instrument ID and On event Class (131)	
36.	Message Identifier (152=Illegal cmd, 153=Parity error, 157=Illegal length, 158=time out, empty=255)	
37.	command ID	
38.	APID	
39.	bit 0,1='00', bit 2..7=PSC(bit2..7)	
40.	PSC (bit 8..15)	
41.	Message #2 Sub instrument ID and On event Class (131)	
42.	Message Identifier (152=Illegal cmd, 153=Parity error, 157=Illegal length, 158=time out, empty=255)	
43.	command ID	
44.	APID	
45.	bit 0,1='00', bit 2..7=PSC(bit2..7)	MSByte
46.	PSC (bit 8..15)	LSByte
47.	Message #3 Sub instrument ID and On event Class (131)	
48.	Message Identifier (152=Illegal cmd, 153=Parity error, 157=Illegal length, 158=time out, empty=255)	
49.	command ID	
50.	APID	
51.	bit 0,1='00', bit 2..7=PSC(bit2..7)	MSByte
52.	PSC (bit 8..15)	LSByte
53.	Message #4 Sub instrument ID and On event Class (131)	
54.	Message Identifier (152=Illegal cmd, 153=Parity error, 157=Illegal length, 158=time out, empty=255)	
55.	command ID	
56.	APID	
57.	bit 0,1='00', bit 2..7=PSC(bit2..7)	MSByte
58.	PSC (bit 8..15)	LSByte
59.	Message #5 Sub instrument ID and On event Class (131)	
60.	Message Identifier (152=Illegal cmd, 153=Parity error, 157=Illegal length, 158=time out, empty=255)	
61.	command ID	
62.	APID	
63.	bit 0,1='00', bit 2..7=PSC(bit2..7)	MSByte
64.	PSC (bit 8..15)	LSByte
65.	Message #6 Sub instrument ID and On event Class (131)	

Register number	Description	
66.	Message Identifier (152=Illegal cmd, 153=Parity error,157=Illegal length,158=time out, empty=255)	
67.	command ID	
68.	APID	
69.	bit 0,1='00', bit 2..7=PSC(bit2..7)	MSByte
70.	PSC (bit 8..15)	LSByte
71.	Message #7 Sub instrument ID and On event Class (131)	
72.	Message Identifier (152=Illegal cmd, 153=Parity error,157=Illegal length,158=time out, empty=255)	
73.	Instrument address (0)	
74.	command ID	
75.	bit 0,1='00', bit 2..7=PSC(bit2..7)	MSByte
76.	PSC (bit 8..15)	LSByte
77.	Message #8 Sub instrument ID and On event Class (131)	
78.	Message Identifier (152=Illegal cmd, 153=Parity error,157=Illegal length,158=time out, empty=255)	
79.	command ID	
80.	APID	
81.	bit 0,1='00', bit 2..7=PSC(bit2..7)	MSByte
82.	PSC (bit 8..15)	LSByte

Table 4: Essential HEPI HK data

An error or overflow in one of the modules rises a flag in the corresponding error register (ref. Table 4). The description of the different flags is listed in **Table 6**. All error flags could be set to 0 individually by command with CID 13 or general by reset, synchronisation and init command.

Bit Number of Error (byte 24 of essential HK)	Modul	Error condition
0	AC	Amplitude correction (overflow of multiplication and addition, underflow of subtraction)
1	LUT	Ratemeters overflow (more then 64535 number of events in one ratemeter cell)
2	MEM	Error overflow histogram (more then 254 number of events in one histogram cell)
3	SPT	Spectral timing overflow . (more then 254 number of events in one histogram cell)
4	TC	Overflow counter zerocrossing CsI events (more then 2^24 -1 wrap over of the 2 sec period. Overflow of zerocrossing counter of CdTe events is not monitored, because both counters could only differ by one digit because of the synchronisation of the detectors
5	MP	Overflow counter of CsI events >10 MeV (more then 2^16 -1 events with more then 10 MeV after last synchronisation, reset, init or clear)

6	CDTE_HBR	Overflow counter CdTe events (more then 2^32 -1 number of events after from last synchronisation, reset, init or clear)
7	CSI_HBR	Overflow counter CsI events (more then 2^32 -1number of events after last synchronisation, reset, init or clear)

Table Fehler! Unbekanntes Schalterargument.**: HEPI Error Flags**

Byte number	Description	default value after HEPI reset	Range
0.	MER threshold of double events	0	MSB ... MSB-7
1.	MER threshold upper threshold of triple events	0	MSB ... MSB-7
2.	MER threshold lower threshold of triple events	0	MSB ... MSB-7
3.	Spectral timing integration time	0	0.9 ... 500 msec
4.	Spectral timing upper threshold (9)	0	MSB ... MSB-7
5.	Spectral timing threshold 8	0	MSB ... MSB-7
6.	Spectral timing threshold 7	0	MSB ... MSB-7
7.	Spectral timing threshold 6	0	MSB ... MSB-7
8.	Spectral timing threshold 5	0	MSB ... MSB-7
9.	Spectral timing threshold 4	0	MSB ... MSB-7
10.	Spectral timing threshold 3	0	MSB ... MSB-7
11.	Spectral timing threshold 2	0	MSB ... MSB-7
12.	Spectral timing lower threshold (1)	0	MSB ... MSB-7
13.	Energy selection lower threshold	0	MSB ... MSB-7
14.	Energy selection upper threshold	16#FF	MSB ... MSB-7
15.	Delay of CsI detector	0	238 nsec – 61 µsec
16.	Delay of CdTe detector	0	238 nsec – 61 µsec
17.	time coincidence acceptance window	0	238 nsec – 61 µsec
18.	On request value HBR I/F A	16#03	MSByte
19.	On request value HBR I/F A	16#E7	SByte
20.	On request value HBR I/F B	16#02	MSByte
21.	On request value HBR I/F B	16#00	LSByte

Table 6: On request HEPI HK data type II (default values)

2.4.2 High bit rate interfaces: HEPI – DPE

HEPI will transmit the scientific data via two HBR I/Fs to the DPE. These two interfaces are different from the one between the detectors and HEPI.
They consist of four lines:

- data (from HEPI)
- enable (from DPE)
- clock (from DPE)
- request (from HEPI to mRTU)

The length of each transmitted character is 16 bit. Each FIFO of HEPI is 8 kword. The clock frequency is 5 MHz (5.242.880 Hz).

The electrical definitions are in agreement with AD.1 and AD.2.
The request lines are connected with the mRTU (relay status).
Table 6 shows an example of an timing scheme of the HBR I/F. Two data words are transmitted. Due to the late high tx_enable signal at each end of a transmission two additional bits of the next word are transmitted. Because the transmission of the accompanying data word is not finished, this data word must be stored and re-transmitted in the next transmission cycle.

Signal	DPE-Side (nsec)		HEPI side (nsec)	
tx_enable ↓	0	0	60 (propagation delay)	60
detection of tx_enable ↓			60 + 95 (half period) (clock ↑)	155
1st bit on line	60 (prop. delay) + 310	370	155 +95 (half period) + 60 (internal delay) (clock↓)	310
sample of 1 bit (b)	2.5 clock cycles after tx_enable	475		
2nd bit on line	60 (prop.) + 500	560	120+ 2*190 (period)	500
sample of 2nd bit	3.5 clock cycles after tx_enable	665		
...	...		...	
16th bit on line	60 (prop.) + 3160	3220	120 + 16*190	3160
sample of 16th bit	17.5 clock cycles after tx_enable	3325		
Reading the output FIFO and loading the shift register with the 2nd data word			60 + 17*190	3230
1st bit of the 2nd data word on the line			60 (internal delay) + 3230	3290
FIFO_WRN	18 clock cycles after tx_enable	3420		
Reading the output FIFO and loading the shift register with the 3rd data word			60 + 33*190	6270
1st bit of the 3rd data word on the line			60 (internal delay) + 3290	6330
FIFO_WRN	34 clock cycles after tx_enable	6460		
tx_enable ↑	34 clock cycles after tx_enable	6460	60 (prop.) + 6460	6520
shift of the 2nd bit of 3rd word to the output			60 + 34*190	6520
detection of tx_enable ↑			60+6460+90 (half period) (clock ↑)	6615
stop of transmission				6615

Table 7: Timing scheme of HBR I/F

2.4.2.1 HBR I/F A

The HBR I/F A will be used to transmit the events, which are not stored inside the HEPI (e.g. photon by photon) and HBR I/F B will be used to readout the histograms.
This requires different definitions of the data packages for these two lines.
HBR I/F A uses two different packages: one short (80 bit) and one long (160 bit). The field definition depends on the event type, but in any case starts with the type field (8 bit). Each value inside the data package is right adjustified.
The MSB will be transmitted first.
An example for a CdTe event in photon by photon mode is shown in Figure 5.

MSB															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
type								rise time							

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
MSB	time since beginning of observation (first 16 bit word)														

32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
time since beginning of observation (second 16 bit word)															LSB

48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
spare					amplitude										

64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
spare	x-position							spare	z-position						

Figure 5: Short data package for events with time information at HBR I/F A

The large data packages are e.g. used by compton events and spectral timing events from CsI. An example for the Compton events is shown in Figure 6.

In normal operational mode either two short (2 ∗ 80 bit) or one long (160 bit) data package (160 bit) is written into the output FIFO (HBR I/F A). This avoids cut off of bits of the data package if a multiple of 160 bit (10 words) is the minimum number of bits, which is transmitted within one transmission cycle of the HBR I/F A.

Table 8 shows a list of the different data types and the corresponding data formats of the HBR I/F A. The numbers corresponds to the transmitted bit numbers, the MSB (bit 0) transmitted first.

Item	HEX Value	Decimal value	Length (80/160)	CdTe /CsI	raw / not raw	Not cal. / cal.	Multiplicity: 01 = single; 10 = double; 11 = triple		Spectral timing	Spare
			Bit 0	1	2	3	4	5	6	7
CdTe single	24	36	0	0	1	0	0	1	0	0
CdTe raw single	04	4	0	0	0	0	0	1	0	0
CdTe raw calibration	14	20	0	0	0	1	0	1	0	0
CdTe cal.	34	52	0	0	1	1	0	1	0	0
CsI single	64	100	0	1	1	0	0	1	0	0
CsI raw single	44	68	0	1	0	0	0	1	0	0
CsI raw double	48	72	0	1	0	0	1	0	0	0

Item	HEX Value	Decimal value	Length (80/160)	CdTe /CsI	raw / not raw	Not cal. / cal.	Multiplicity: 01 = single; 10 = double; 11 = triple		Spectral timing	Spare
multiple										
CsI raw triple multiple	4C	76	0	1	0	0	1	1	0	0
CsI raw single calibration	54	84	0	1	0	1	0	1	0	0
CsI mult.	68	104	0	1	1	0	1	0	0	0
CsI single and CdTe	A4	164	1	0	1	0	0	1	0	0
Calibration: CsI single and CdTe	B4	165	1	0	1	1	0	1	0	0
CsI mult. and CdTe	A8	184	1	0	1	0	1	0	0	0
Spectral. timing	E6	246	1	1	1	0	0	1	1	0

Table 8: Type definition and format of HRB I/F A

Item	Type field	Rise time	Event time	Amplitude	Y-Pos.	Z-Pos.	Amplitude	Y-Pos.	Z-Pos.	Spare	Total length
CdTe single	0-7	8-15	16-47	53-63	65-71	73-79					80
CdTe raw	0-7	8-15	25-47	53-63	65-71	73-79					80
CdTe cal.	0-7	8-15	16-47	53-63	65-71	73-79					80
CsI single	0-7		16-47	54-63	66-71	74-79					80
CsI raw	0-7		25-47	54-63	66-71	74-79					80
CsI mult. *1)	0-7		16-47	54-63	66-71	74-79					80
CsI single and CdTe *3)	0-7	8-15	16-47	53-63 CdTe	65-71 CdTe	73-79 CdTe	86-95 CsI	98-103 CsI	106-111 CsI	112-159	160
Calibration: CsI single and CdTe *3)	0-7	8-15	16-47	53-63 CdTe	65-71 CdTe	73-79 CdTe	86-95 CsI	98-103 CsI	106-111 CsI	112-159	160
CsI mult. and CdTe *2)	0-7	8-15	16-47	53-63 CdTe	65-71 CdTe	73-79 CdTe	86-95 CsI	98-103 CsI	106-111 CsI	112-159	160
Spectral. Timing	0-7		16-47	48-111 (8 histograms with 8 bit width)						112-159	160

Table 9: List of data type and formats of the HBR I/F A

*1): For CsI multiple events in case of polarimetric events (double events with position of second event in direct neighbourhood) following bits are set additionally with polarimetric information:

Bit No	8	9	10	11	12	13	14	15
	0	0	0	1	0	Pol Dat		

*2): For Compton multiple events in case of CsI polarimetric events (double events with position of second event in direct neighbourhood) following bits are set additionally with polarimetric information:

Bit No	80	81	82	83	84	85
	0	Pol Dat			1	0

*3): For Compton events additional bits in the data field indicates, if only CdTe, CsI or both events are calibration. In the last case, also the calibration flag (bit 3) of the event header will be set.

Bit No	50	51
	CdTe Calibration	CsI calibration

MSB															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
type								rise time							

16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
MSB	time since beginning of observation (first 16 bit word)														

32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
time since beginning of observation (second 16 bit word)															LSB

48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
spare					amplitude CdTe										

64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
spare	x-position CdTe							spare	z-position CdTe						

80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
spare	Dat Pol			Pol		amplitude CsI									

96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
spare		x-position CsI						spare		z-position CsI					

112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
spare															

128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
spare															

144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
spare															

Figure 6: Example of a long data package format of events with time information at HBR I/F A

2.4.2.2 HBR I/F B

HBR I/F B transmits the content of the mass memory (except the LUT).
HEPI put the data from the memory from start-address to stop-address after a DPE-IASW command to the line. Start-address and stop-address are parameters of the command.
Figure 7 shows the data format of the HBR I/F B. Data - Block length is 1kbyte.

Byte								
0	1	2	3	4	5	...	1024	1025
Start Address/ 1024 MSByte	Start Address/ 1024 LSByte	Data byte start+0	Data byte start+1	Data byte start+2	Data byte start+3		Data byte start+1022	Data byte start+1023

Figure 7: Data format of HBR I/F B

2.4.3 ON/OFF line

An ON/OFF (7) line from DPE to HEPI is used to initialised HEPI.

2.4.4 HEPI Status line

A status line between HEPI and DPE indicates via DPE relay status read out, if the 4 MHz and the 1 sec pulse is distributed to from DPE to HEPI. The output of the status line is a 1 Hz clock. It could be used for diagnostic purposes, if LBR commands are not working.

2.5 Interfaces HEPI – detectors

2.5.1 High bit rate interface HEPI – detectors

The fast serial line interface transmits scientific data from the detectors to the HEPI in only one direction. Synchronisation information is transmitted to the detectors from HEPI.
It consists of six differential twisted lines:

- data (from detector)
- sample (from HEPI)
- FIFO not empty (from detector)
- clock (from HEPI)
- synchronisation (from HEPI)
- clear FIFO (from HEPI)

These six lines control the data transmission and timing via hardware handshaking. The clock frequency is 4,194,304 Hz and should be synchronous to the system clock.
The length of each transmitted word is 64 bit and consists of four 16 bit sub words.
1st word: Time in units of 238.4 ns (most significant 16 bit of 24 bit time word)
2nd word: 8 bit Time (least significant 8 bit of 24 bit time word) plus
8 bit Rise Time (only applicable for CdTe)
3rd word: 11 bit Amplitude (CdTe 11 bit, CsI 10 bit) plus 1 bit flag for CdTe Calibration or plus 2 bit flags for CsI calibration and multiple event, plus 2 bit for number of multiple events
4th word: Pixel Address (CdTe 14 bits, CsI 12 bits)
The pixel address of the individual pixel is: Y value (6 bit for CsI or 7 bit for CdTe) and Z value (6 bit for CsI or 7 bit for CdTe).

The data are right adjustified, where applicable. The LSB of information is the LSB of a 16 bit word. The transmitted sequence of the words is 1,2,3,4. The MSB is transmitted first.

1st word

MSB															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
time 1st byte (MSB)								time 2nd byte							

2nd word

16	17	18	19	20	21	22	23	24	25	260	271	282	29	30	31
time 3rd byte (LSB)								rise time (only CdTe)							

3rd word

32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
cal. flag					amplitude (CdTe)										
cal. flag	mmc	pulse ID		MUX		amplitude (CsI)									

4th word

															LSB
48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
		address (CdTe)													
				address (CsI)											

Figure 8: Format of data packages from the detectors to HEPI (mmc: multiple module coincidence 1 true, 0 no MMC; pulse ID: order of the pulse in a multiple event with possible values 00 first event, 01 second event, 10 third event; MUX: Multiplicity with possible values 00 MUX 1, 01 MUX 2, 10 MUX 3)

2.5.2 Timing of the data transmission of the HBR I/F between the detectors and HEPI

If the FIFO_not_empty line is high HEPI generates the sample pulse on the falling edge of the clock pulse to get the next data word. On the next rising edge of the clock pulse [1] (the numbers corresponds to Figure 9) the source (IFDM or PFDM) writes a new data word from the detector FIFO to the output shift register. Due to the propagation delay of the lines and the drivers the clock pulse at the detector is delayed between 8 and 60 nsec. This is also true of the data, i.e. the first data is after max. 60 nsec at the HEPI input register. If the data word was the last data word in the output FIFO the FIFO_not_empty [FIFO NE] line should go low within the next TBD nsec.

On the next rising edge of the clock pulse [2] HEPI shifts one bit from the RS 422 receiver to the input shift register (HEPI gets DATA-new-1). At this time the output register shifts the next bit to the RS 422 driver. Then, on the next rising edge [3] HEPI shifts this bit into its input register and so on.

If the FIFO_not_empty line is still high and HEPI is also ready for read in, HEPI generates a new sample pulse with the falling edge of the 64th clock pulse from the beginning. With the next rising edge [65] HEPI reads the last bit (64th) of the previous data word in and the source

writes the next data word to the output shift register and the transmission continues. With the next falling [65] edge of the clock pulse, i.e. after complete a transmission of one data word (64 bit), HEPI reads the data from the input shift register.
If the FIFO_not_empty line is not high, HEPI generates no new sample pulse and reads only the data word from the input shift register.
With the rising edge of the clock pulse HEPI clears the output FIFOs. The clear FIFO lines from HEPI to the detectors goes low. The pulse width of the FIFO reset pulse is one DPE clock cycle (234 nsec) (not shown in Figure 9).

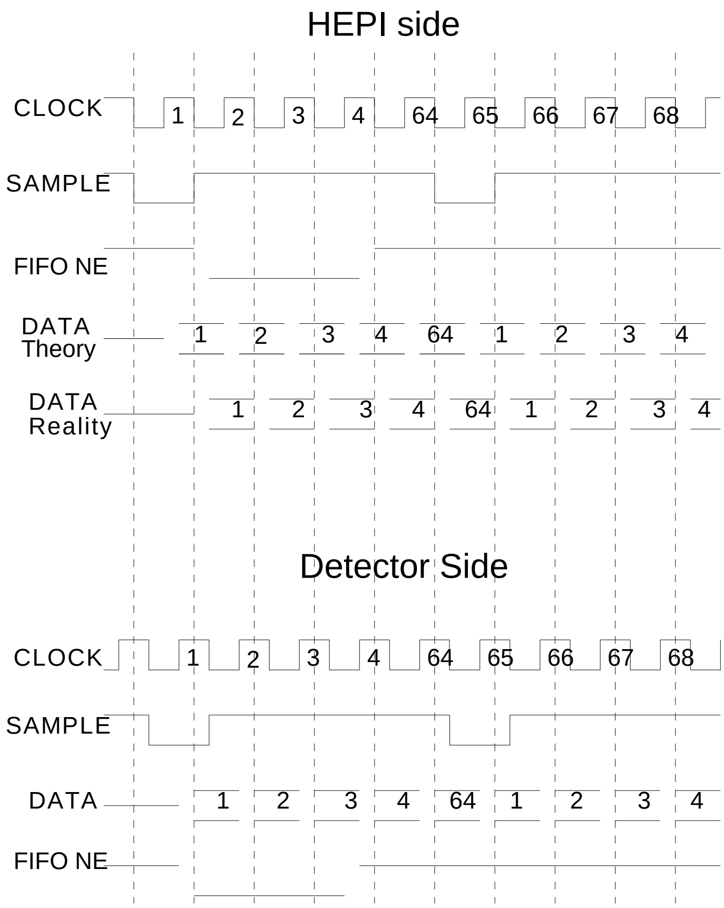

Figure 9: Timing scheme of HBR I/F between detectors and HEPI

2.6 Electrical Characteristics

2.6.1 Harness

The two boards are connected with 80 pin connectors inside the frame. The main board (lower board) gets the power, the clock and synchronisation pulses via a connector from the back plane.

On the front side are four connectors. Two of them are connected with the detector layers, two with the DPE.

Subsystem	to/from	Connector type	Connector Name
HEPI LBR I/F DPE, status	DPE LBR I/F, mRTU	DAMA 26 S (high density)	HEPI_J19
HEPI HBR I/F DPE, clock, sync.	DPE	DAMA 26 S (high density)	HEPI_J18
HEPI HBR I/F CdTe detector	CdTe detector	DAMA 26 S (high density)	HEPI_J16
HEPI HBR I/F CsI detector	CsI detector	DAMA 26 S (high density)	HEPI_J17
HEPI power supply	DPE	HE 801-17 P	HEPI_J1
HEPI board interconnection Main board	HEPI Memory board	HE 801-53 S	HEPI_J2
HEPI board interconnection Memory board	HEPI Main board	HE 801-53 P	HEPI_J3

Table 10: Listing of connectors used by HEPI

2.6.2 Shielding philosophy

2.6.2.1 Shielding of the detector HBR I/Fs

Each input and output to and from detectors is realized as a differential RS-422A interface. The layout of the shielding of individual lines is shown in Figure 10.

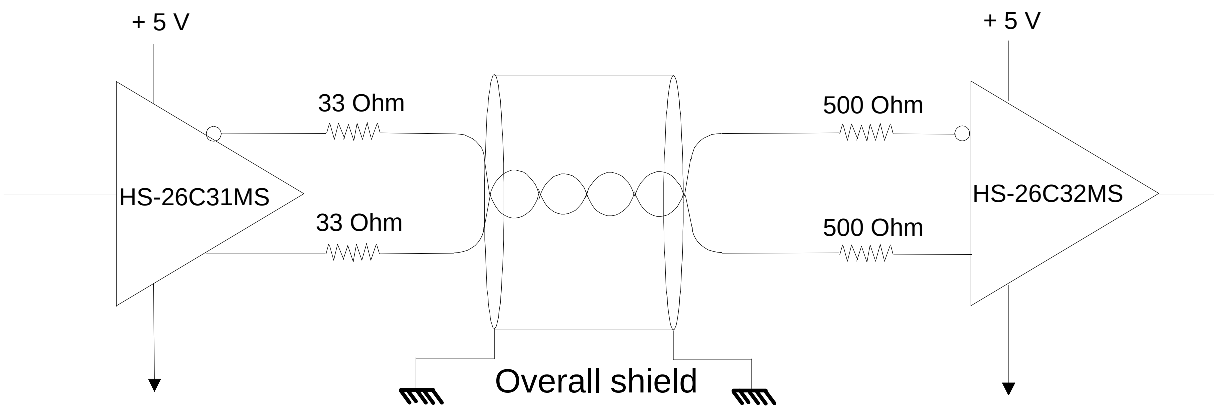

Figure 10: Shielding philosophy of a RS-422A interface

2.6.2.2 Shielding of the DPE I/F

The shielding of the interface lines between the DPE and HEPI is in according with AD.1.

3 Engineering requirements

3.1 Power allocation

HEPI power allocation at 5V is:

Stand by mode:	160 mA	0.8 W
Nominal mode:	160 mA	0.8 W
Initialisation (for 4sec):	200 mA	1.0 W

3.2 Power dissipation

Power dissipation is similar the power allocation:

Stand by mode:	0.8 W
Nominal mode:	0.8 W

3.3 Electronic layout

HEPI is configured out of two PCBs. The two boards are connected with an internal connector.
The FPGA or ASIC is placed on the main board.
The front connectors are also connected to the main board.
The memory board contains only parts of the memory (3 Mbyte).
Figure 11 shows the HEPI frame with connectors and PCBs (upper part).

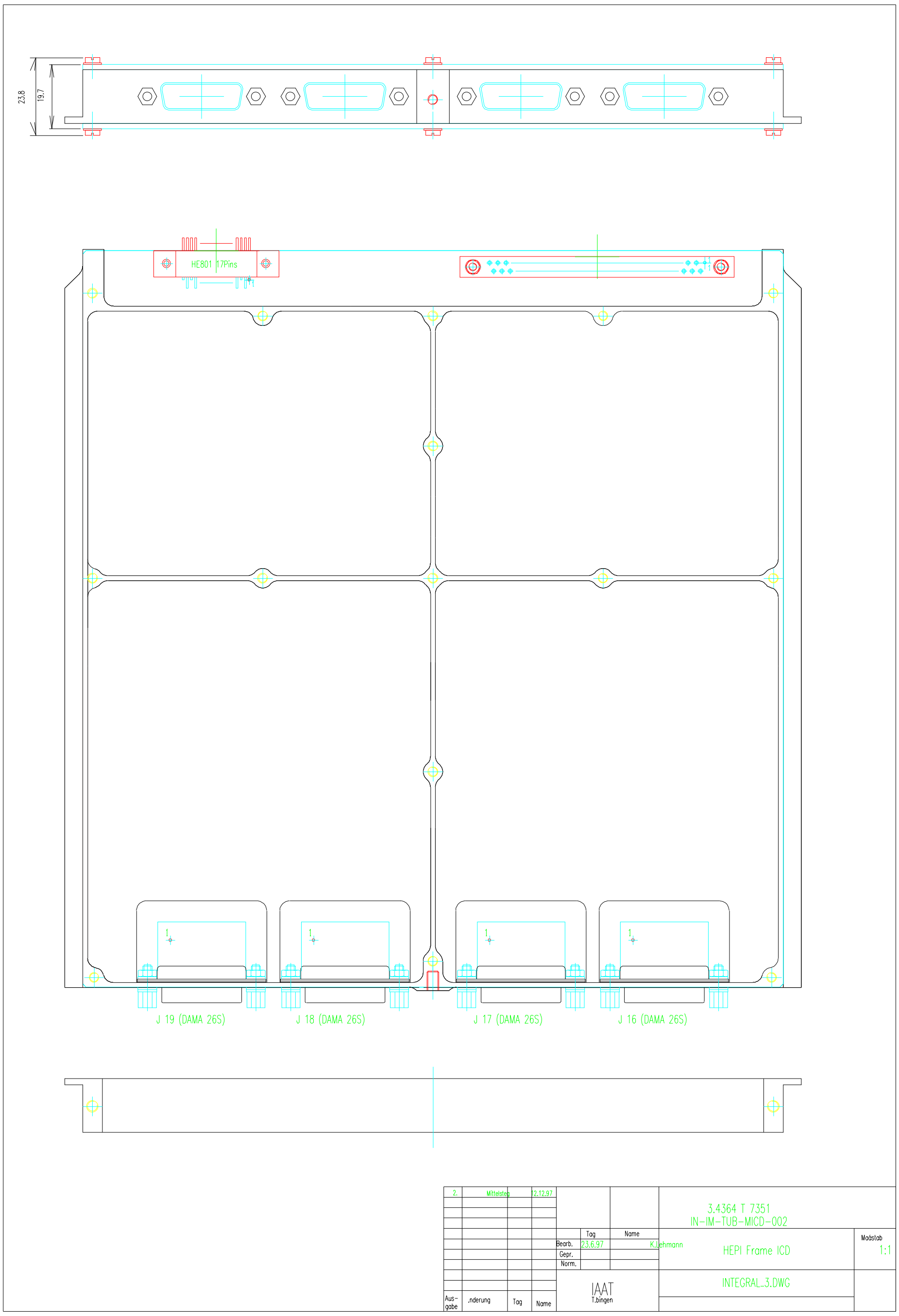

Figure 11: HEPI with connectors and mounted boards

3.4 Dimensions

Table 11 lists the dimensions of the two boards and the module.

	Board	Frame
Length:	225	227.5
Width:	214	226
Height:		16.2 (without PCB's)

Table 11: Dimensions of the HEPI boards and frame

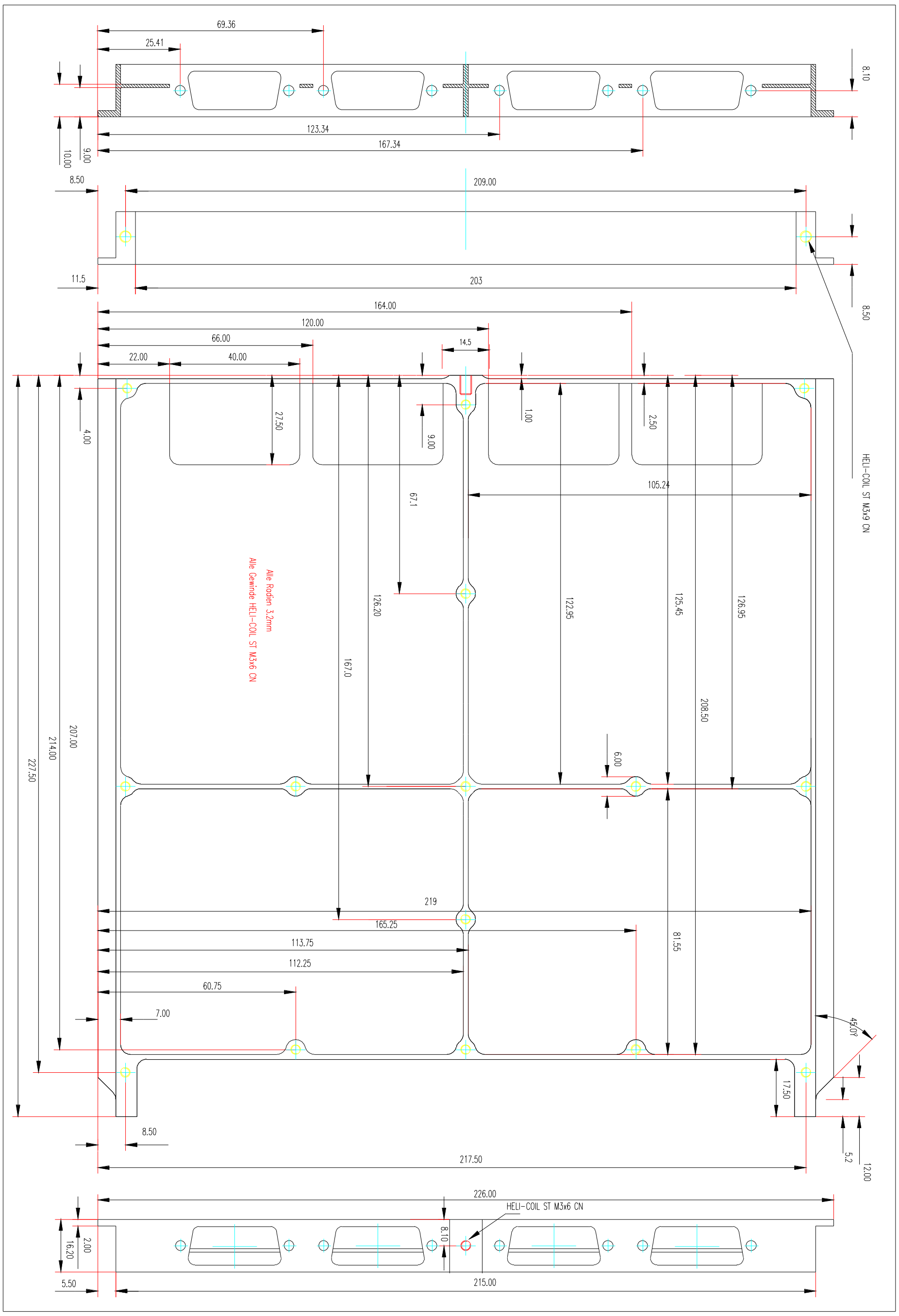

Figure 12 : Mechanical drawing of the HEPI module.

3.5 Mass allocation

HEPI requires following mass allocation

2 Boards (a 400 g)	800 g
Connectors, screws, etc.	200 g
1 Module	280 g
	1280 g
margin 15 %	+192 g
total	1472 g

All elements on the board will be well pro-portioned placed on the board.

3.6 Thermal design

The temperature of the PCB at boundary conditions of +40 °C is about 55 °C nominal power and 50 °C with standby power.
(cf. PG/10.3.2/RT/1905/rt)