
Design and implementation of an
FPGA-driven, hardware-based
realtime data reduction system for
pixelated photon detectors

DIPLOMARBEIT

von

Stefan Dennis Christmann

am

Institut für Astronomie und Astrophysik
Eberhard Karls Universität Tübingen

Tübingen

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Die vorliegende Arbeit widme ich meinen Eltern **Hermann und Cornelia Christmann**, ohne deren Hingabe und Aufopferung ich nicht der Mensch sein könnte, der ich heute bin.

Danke dafür, dass ihr alles tut, damit ich meine Träume verfolgen und mein Leben erfolgreich gestalten kann. Ich könnte mir keine besseren Eltern wünschen und bin unendlich dankbar für all das, was ihr mir gegeben habt.

Dieses erfolgreich abgeschlossene Studium ist auch euer Verdienst!

Deutsche Zusammenfassung

Weltraumbasierte Röntgenobservatorien wie das *International X-ray Observatory* (IXO) sind mit einer Vielzahl unterschiedlicher Messinstrumente ausgestattet, die durch ihre hohen dynamischen Messbereiche und Bildraten mehrere Gigabyte an Daten pro Sekunde generieren können. Oftmals werden sie dafür in einen Orbit um den Lagrange-Punkt L2 gebracht, der ca. 1.5 Millionen Kilometer von der Erde entfernt liegt, thermisch sehr stabil und fast kräftefrei ist. Ein großer Nachteil ist seine weite Entfernung zu den terrestrischen Bodenstationen und die dadurch stark limitierte Übertragungsbandbreite, die ohne weitere Maßnahmen von der Menge der Messdaten weit überschritten wird. Es ist jedoch möglich, die in den Messdaten enthaltenen Informationen bereits auf dem Satelliten zu extrahieren und danach auf wissenschaftliche Relevanz hin zu untersuchen. Begünstigt durch die geringen Photonenflussraten vieler interessanter Quellen kann man somit einen Großteil irrelevanter Datenpakete verwerfen und im Rahmen der verfügbaren Bandbreite arbeiten.

Die vorliegende Diplomarbeit beschäftigt sich mit der Entwicklung und der Implementierung eines *Event Pre-Processors* für pixelbasierte Photonendetektoren, der aufgenommene Informationen auf wissenschaftliche Relevanz hin untersucht und markiert. Anhand des *Wide Field Imagers*, einem Photonenspektrometer auf DEPFET-Basis für die IXO Mission, wird gezeigt, wie eine solche Hardware in Echtzeit und bei sehr hohen Bildwiederholungsraten (1000 Bilder pro Sekunde) arbeiten und spezielle Eigenschaften von Field Programmable Gate Arrays ausnutzen kann, um die notwendigen Analyseschritte in nur wenigen Nanosekunden durchzuführen.

Die durchgeführten Arbeiten stellen eine Weiterentwicklung des bereits bestehenden Konzeptes des D3C Event Pre-Processor dar, der von Thomas Schanz für die Simbol-X Mission entworfen wurde. Mit Hilfe zusätzlicher Implementierungen im Rahmen dieser Diplomarbeit, wie der erstmaligen Hardwareumsetzung des *Odd-Even Transposition Sortieralgorithmus* auf einem Virtex4 SX-35 FPGA, war es somit möglich, das Konzept von der VHDL Planungsphase bis hin zum ersten funktionsfähigen Hardwareprototypen zu realisieren. Abschließende Tests in Hard- und Software zeigten dabei bereits eine hohe Reife des Entwurfs und legen den Grundstein für eine erfolgreiche Weiterführung des Projekts.

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1 Introduction

In search of the origin of our existence, astronomy has always been an important field of studies and the utilization of telescopes with focussing optics by Galileo Galilei¹ in the early 17th century was one of the biggest leaps in astronomy, which ever occurred. Nowadays, the word telescope is used to describe a broad variety of sophisticated instruments and detectors, which are used to detect photons throughout the electromagnetic spectrum or even highly energetic particles, which can carry information from the interior of stars or the depth of the Universe.

Many of these detectors have completely different functionalities, but all of them produce large amounts of data, which can only be stored and analyzed with the help of powerful computers. While this does not present a problem for ground-based observations, where computers can be connected in large-scale clusters or worldwide computing networks, satellite-based missions only have limited computing and storing capabilities and need to transfer data to the ground, before it can be processed. Furthermore, they are equipped with multiple data-generating instruments, while at the same time only having limited bandwidths for data-transfer. Consequently, the size of the raw-data stream needs to be reduced onboard the satellite itself, in order to allow the transmission of relevant scientific information to the ground.

This thesis deals with the topic of onboard, realtime event pre-processing for pixelated photon detectors and the design of hardware, which can be used to analyze the scientific importance of their data. It will present a solution to the highly time-critical and efficient data-reduction needs of the *Wide-Field Imager* (WFI), which is a pixel-based X-ray imaging device onboard of the proposed next large-scale X-ray space telescope, the *International X-ray Observatory* (IXO). It will furthermore focus on modern-day electronics development and present promising results of a first working *Event Pre-Processor* (EPP) prototype, which was designed in the framework of this thesis. Further details about the mission and the involved electronics will be presented in Chapter 3 and 5 respectively, while an overview over the essential physics of X-ray astronomy will be given in the following sections.

1.1 Astronomical Windows

The field of astronomy is very dynamical and driven by science and technological improvements of various types. The development of new detectors with improved *quantum efficiencies* and high *Signal-to-Noise Ratios* (SNR), allows scientists to detect and record data from very faint sources. Especially the class of *photon detectors* has profited from advances in the past decades and covers detectable energy ranges throughout the whole electromagnetic spectrum.

¹Galileo Galilei (*1564, †1642) was an Italian scientist, who can be considered the founder of modern science, in which empirical studies and observations lead to laws, which can be tested and refined by further measurements.

Some of these ranges are grouped together (as shown in Figure 1.1) and are commonly referred to as *astronomical windows*. Within these windows, many successful missions have delivered terabytes of valuable data and have shaped our understanding of the Universe and the processes involved in its evolution.

Currently, astronomy is entering a very exciting new era, as new astronomical windows are opened by the proposal of new types of missions, in order to overcome the limitation of using electromagnetic photons as carriers of information and to shed light on processes and objects, that do not interact electromagnetically. The most prominent development in this ongoing paradigm-shift is the increasing importance of particle physics for astronomy, as both fields are slowly merging together into a common field called *astroparticle physics*.

Observations within these new windows promise to deliver insights into exotic places of the Universe, like the interior of the Sun for example. *Neutrinos*, which are created in reaction chains of solar fusion processes, can escape the Sun's interior with almost no interaction whatsoever and still carry information about their spatial origin. By building very sensitive *neutrino telescopes* (in order to increase the detection efficiency of these particles) the field of *neutrino astronomy* could enlarge the current understanding of stars, their evolution and inner structure significantly.

Additional to astroparticle physics, the window of gravitational waves might be opened by missions like the *Laser Interferometer Space Antenna* (LISA) in the near future. Ground-based gravitational wave experiments have been conducted for around 20 years (LIGO², GEO 600³, etc), but have mainly been unsuccessful due to the interference of their surroundings and their limitations in maximum base-length. These problems could be avoided, by moving necessary detectors into space, therefore making LISA a necessary next step, in order to progress the evolution of this very young field.

All of the aforementioned missions will look at objects on the celestial sphere. Contrary to this, the JEM-EUSO⁴ experiment will do the exact opposite. Its telescope, which can detect UV photons, will be mounted on the *International Space Station* (ISS) and look down onto Earth, surveying particle events in its atmosphere and gathering information about their origin, energy and type. In fact, it will use large portions of our atmosphere as a particle detector.

Lastly, experiments like CRESST⁵ and DAMA⁶ will deliver new information about the existence of *dark matter*, and the role it played for structure formation of the early Universe. This non-baryonic matter only interacts gravitationally and via the weak-force and can not

²Laser Interferometer Gravitational Wave Observatory.

³German Gravitational Waves Detector, based on Michelson interferometer, close to Hannover.

⁴Extreme Universe Space Observatory, which will be attached to the JEM (Japanese Experiment Module) Module on the ISS.

⁵Cryogenic Rare Event Search with Superconducting Thermometers, European Dark Matter experiment in the Italian Gran Sasso underground laboratory.

⁶Dark MATter, Italian dark matter experiment, also located at the underground laboratories at Gran Sasso, Italy.

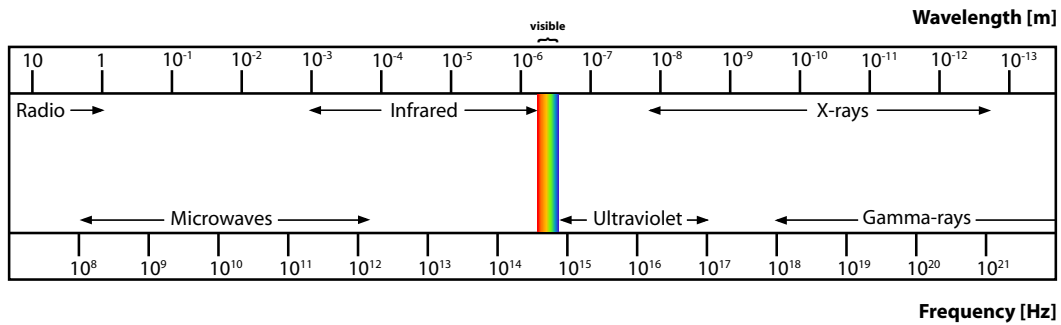


Figure 1.1: The electromagnetic spectrum spans a wide range of wavelengths and frequencies, as shown in the figure above. However the optical, or visible part of the spectrum, just accounts for a very small fraction of photon energies. The development of new detectors which can detect photons throughout the whole electromagnetic spectrum has therefore increased the amount of information we can gather about celestial objects. (Gandhi, 1997)

be detected directly through any of the currently opened astronomical windows. Gaining more knowledge about its origin and properties will move us back further along the timeline leading to the events close to the big bang and reveal more information about the origin of the Universe.

1.2 The Origins of X-ray Astronomy

One of the electromagnetic windows that remained closed to astrophysicists for a long time was the energy region of X-ray radiation. Since X-rays cannot penetrate our atmosphere completely (see Figure 1.2), detecting X-ray photons is not possible with ground-based telescopes. The first successful attempt to do X-ray astronomy was undertaken in 1962. During a rocket-flight, where scientists were trying to detect X-ray photons originating from the moon's surface, Giacconi⁷ et al. discovered the first extra-solar X-ray source, *Scorpius X-1* (Sco-X1) (Giacconi et al., 1962). This groundbreaking discovery triggered an era of X-ray missions and many balloon experiments, transporting X-ray detectors to altitudes in the atmosphere, where a sufficient X-ray flux still exists. It became obvious however, that one major disadvantage - the limitation of observation time from a few minutes up to a few hours - could not be overcome this way.

A solution to this problem was presented with the start of the *Uhuru*⁸ satellite in 1970, which was the first X-ray satellite ever launched. While surveying the sky for more than two years, Uhuru discovered a total of 339 X-ray sources, further intriguing astronomers about the field of X-ray astronomy. (Forman et al., 1978)

With the utilization of grazing incidence Wolter-I type telescopes (energy range of 0.1 - 4 keV) on the *Einstein* satellite, which was operational from 1978 until 1981, it became possible to

⁷Riccardo Giacconi (*October 6th, 1931) is an Italo-American physicist, who received the Nobel Prize for his extraordinary astrophysical work, that led to the discovery of cosmic X-rays.

⁸The Swahili word for freedom.

perform imaging of known X-ray sources and to study extended objects like *supernova remnants*. Moreover it was now possible to resolve many extragalactical X-ray sources in the *Andromeda Galaxy* and the *Large Magellanic Cloud* (LMC). (NASA, 2011a)

Following Einstein, the *European Space Agency* (ESA) launched the *European X-ray Observatory Satellite* (EXOSAT) mission in 1983, which was operational until 1986. During this timeframe it made 1780 observations of objects like *Active Galactic Nuclei* (AGN), *stellar coronae*, *cataclysmic variables*, *X-ray binaries*, *clusters of galaxies* and *Supernova remnants*. With its large sensitivity range of 0.05 - 50 keV, EXOSAT was able to discover the first quasi periodic oscillations in *Low Mass X-ray Binaries* (LMXBs) and *X-ray pulsars*. (NASA, 2011a) The first imaging X-ray survey of the sky was performed in 1990, when the German/US/UK mission ROSAT⁹ was launched. It operated for almost nine years and even though it was only sensitive to a small fraction of the X-ray band (0.1 - 2.5 keV), it extended the catalogues of known X-ray sources to more than 150000 entries during the first six months of the mission. (NASA, 2011a)

In 1996 an Italian-Dutch mission called *BeppoSax* was launched and operated for six years, extending the sensitive energy range up to 300 keV. For the first time in history of X-ray astronomy, astronomers were able to observe highly energetic events like the afterglow of *Gamma-ray bursts* with arcminute precision. Furthermore, BeppoSax enabled scientists to perform wide range spectroscopic investigations of many X-ray sources. (NASA, 2011a)

Approximately 40 years after the launch of Uhuru, the field of X-ray astronomy has become a very important tool in modern astronomy, revealing information about hot ($> 10^6$ K) and exotic objects in the Universe. Current missions like the very successful *Chandra* and *XMM-Newton* X-ray space telescopes, which were both launched in 1999, have delivered terabytes of valuable data and continue to do so. As we begin to barely understand these highly energetic objects and their connections to the origin of the universe, new profound questions arise and new theories have to be formulated. In order to answer these questions and prove those theories, many new missions like IXO have been proposed. Before focussing on the future of X-ray astronomy however, an overview of the physical processes, which are essential for the creation of X-ray photons and their interaction with matter, will be given.

1.3 Physical Processes of X-ray Creation

As mentioned in the previous sections, X-rays are located in the more energetic part of the electromagnetic spectrum (wavelengths $10^{-8} - 10^{-13}$ m). Processes, which are able to produce X-ray photons are separated into two main categories - thermal and non-thermal. Scientists often use the terminology of thermal or non-thermal radiation in order to state how the corresponding photons were created. Unless denoted otherwise, the following sections are mainly based on Carroll and Ostlie (2007) and Unsoeld and Baschek (2005).

1.3.1 Thermal Radiation

Blackbody Radiation

The most important thermal process for photon creation is *blackbody radiation*. A blackbody is an idealized object, which acts as a perfect absorber and does not reflect or transmit any

⁹ROentgen SATellit.

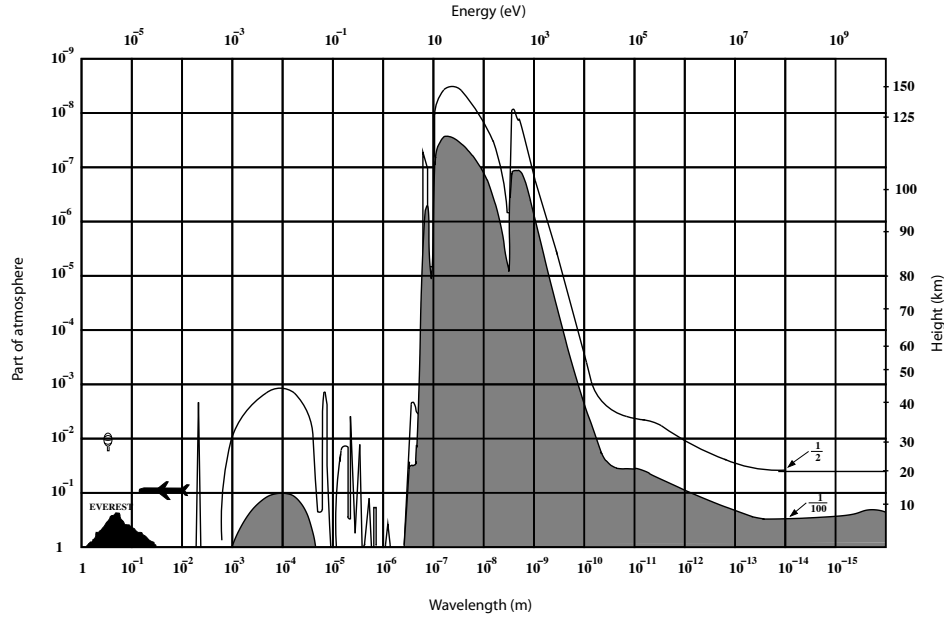


Figure 1.2: The plot shows how electromagnetic radiation is absorbed in the Earth's atmosphere. The upper curve shows the height in which 50% of the incoming radiation is absorbed. The lower curve shows the height in which 99% of radiation is absorbed. For the X-ray band (wavelengths $10^{-8} - 10^{-13}$ m), all incoming radiation is absorbed about 15 km above ground, making it impossible to realize ground-based X-ray astronomy. (Giacconi, 1968)

incident radiation. It is supposed to be in perfect thermodynamical equilibrium and does not exchange any thermal energy with its surroundings. Light, which is emitted from a blackbody, can therefore only be caused by its temperature T , making it the only variable, which is needed to describe its spectrum. The *Planck*¹⁰ formula describes the intensity I of light with frequency ν , which is emitted by a blackbody.

$$I(\nu, T) = \frac{2h\nu^3}{c^2} \cdot \frac{1}{\exp\left(\frac{h\nu}{k_B T}\right) - 1} \quad (1.1)$$

In this equation, k_B is the *Boltzman*¹¹ constant, h is the *Planck constant* and c the speed of light in vacuum.

If plotted versus ν , the intensity I will have a maximum at a distinct frequency (see Figure 1.3). This frequency will change with a variation of T , creating a connection between the frequency of highest intensity and the temperature. This relation allows to derive the surface temperature of a blackbody with a given spectrum. Mathematically, this can be achieved by using the *Wien*¹² displacement law, which expresses the frequency ν_{\max} of highest intensity

¹⁰Max Karl Ernst Ludwig Planck (*1858, †1947) was a German theoretical physicist and recipient of the Nobel Prize for physics in 1918. He made major contributions to the field of quantum mechanics.

¹¹Ludwig Boltzmann (*1844, †1906) was an Austrian physicist and philosopher, who made major contributions in the field of thermodynamics.

¹²Wilhelm Carl Werner Otto Fritz Franz Wien (*1864, †1928) was a German physicist and recipient of the Nobel Prize for physics in 1911.

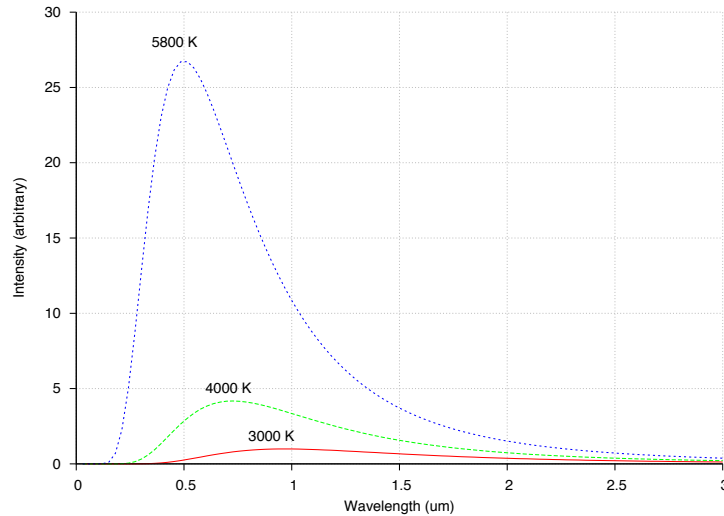


Figure 1.3: The plot shows blackbody spectra for different surface temperatures. A temperature of 5800 K is a good approximation for the blackbody spectrum of our Sun and shows how the energy of maximum emission moves to decreasing wavelengths for increasing surface temperatures.

as a function of T .

$$\nu_{\max}(T) = 5.878933 \cdot 10^{10} \frac{\text{H}}{\text{K}} \cdot T \quad (1.2)$$

A blackbody, which emits the major part of its light within the X-ray band (approx. 0.1 - 50 keV) therefore has to have a high surface temperature of $10^6 - 6 \cdot 10^8$ K.

Bremsstrahlung

A second important process for the creation of thermal radiation is *bremsstrahlung*, which is derived from the German verb "bremsen" and means slowing down. This terminology however, has merely historical background and was first used by Wilhelm-Conrad Röntgen¹³, who was the first scientist to artificially create X-rays by accelerating electrons from an anode to a cathode where they were stopped abruptly by the cathode material. It is important to note, that bremsstrahlung is not only created if charged particles are slowed down, but generally, if they are accelerated. If the acceleration is caused by an electrical field, the emitted radiation is called bremsstrahlung. If the particles are deflected in their trajectory by a magnetic field, the resulting radiation is called *synchrotron radiation*, which will be further explained in Section 1.3.2. The main sources for bremsstrahlung are hot plasmas, where free electrons are accelerated/decelerated by local electric fields of atomic nuclei. In such hot gases it is common to assume a Maxwell¹⁴-Boltzmann velocity-distribution for the constituent particles,

¹³Wilhelm Conrad Röntgen (*1845, †1923) was a German scientist. He discovered X-rays in 1895 and was awarded the Nobel Prize for physics in 1901.

¹⁴James Clerk Maxwell (*1831, †1879) was a Scottish physicist, who formulated the Maxwell-equations for modern electrodynamics and merged the two fundamental phenomena of electricity and magnetism into

which leads to a continuum spectrum of bremsstrahlung radiation. The emission intensity at a certain energy can be described by

$$I(E) \sim (k_B T)^{-\frac{1}{2}} \cdot \exp\left(-\frac{E}{k_B T}\right) \quad (1.3)$$

and therefore decreases quickly at high energies. This drop is also called an *exponential cut-off*.

Characteristic Radiation and Fluorescence

Characteristic radiation occurs, if a free electron interacts with a bound electron in a low energy shell of an atom. If the energy of the incident electron is higher than the binding energy of the bound electron, it is possible, that the bound electron is removed from the atom, leaving it ionized with a vacant energy state. These states are usually denoted by their main quantum number n , where $n = 1$ defines the lowest shell (K-shell) with highest binding energy. Electrons from higher shells ($n = 2, 3, 4, \dots$) or free electrons can now fill the vacant state, generating a more stable configuration of the atom. If such a transition occurs, the energy difference between the incident electron and the vacant shell is emitted as a photon, which is called a *characteristic photon*. For a bound-bound transition, this energy is discrete and will show up as a distinct line in the emission spectrum. Moreover, energy differences between bound states are unique for each atom, thus leading to a corresponding line spectrum, which can be used to determine the specific sort of the atom. In order to classify all these lines, a simple system of a letter and a Greek subscript is used. Every transition ending in the K-shell for example is part of the *K-series*. The origin of the transition is denoted with α if it was the neighboring shell, β for the next higher shell, and so on. A transition of an electron from the L- into the K-shell is therefore called a K_α transition (see Figure 1.4).

It has to be added, that not only electrons are capable of ionizing a neutral atom in one of its lower energy shells, but also photons of sufficient energy. In this case, radiation which is caused by the atomic transition is called *fluorescence* or *fluorescent radiation*. One line of high astrophysical relevance is the 6.4 keV K_α fluorescence line of neutral iron, which can also be used to measure rotational velocities of compact objects for example.

1.3.2 Non-thermal Radiation

Synchrotron Radiation

The trajectories of charged particles in magnetic fields are altered in a very characteristic way by the Lorentz¹⁵-force, which is given by the equation

$$\mathbf{F}_L = \frac{q}{c} \cdot (\mathbf{v} \times \mathbf{B}) \quad (1.4)$$

where q is the charge and \mathbf{v} the velocity of the particle and \mathbf{B} the magnetic field. The equation shows, that \mathbf{F}_L is always perpendicular to \mathbf{v} and \mathbf{B} and therefore does not change $|\mathbf{v}|$, but only its direction. If a moving particle has a velocity component perpendicular to \mathbf{B} , the Lorentz-force will accelerate it constantly, forcing it onto a helical orbit around the direction

one common discipline.

¹⁵Hendrik Antoon Lorentz (*1853, †1928) was a Dutch physicist and recipient of the Nobel Prize for physics in 1902.

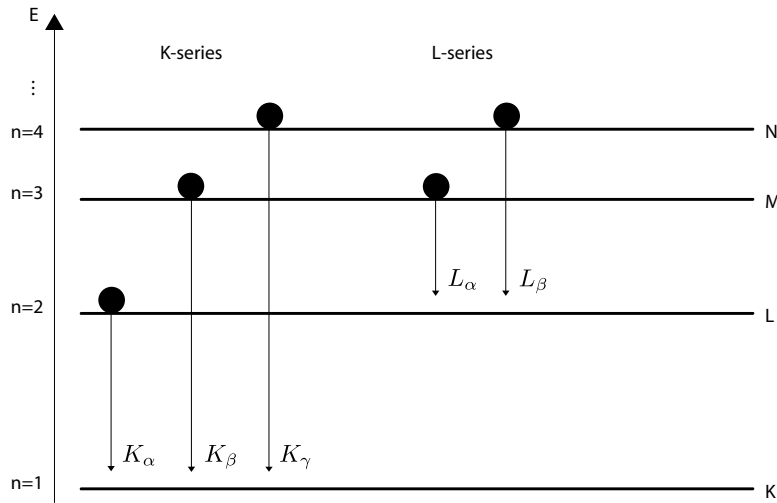


Figure 1.4: The possible energy levels for electrons in an atom are labeled with $n=1, 2, \dots$ or K, L, ... accordingly. Electronic transitions from higher to lower energy states are always labeled with the letter of the shell they end in. The Greek subscript denotes the shell that they originated from. To serve as examples, some transitions from the K- and L-series are shown.

of the magnetic field lines. Identical to the process of bremsstrahlung, the charged particle will emit radiation, which is called *synchrotron radiation* in this case. Its energy is dependent on the strength of the magnetic field, the charge of the particle and its velocity. The frequency of the radiation can be calculated by

$$\nu_{\text{syn}} = \frac{3\gamma^2 qB}{4\pi mc} \quad (1.5)$$

where m is the mass of the particle and $\gamma = \frac{1}{\sqrt{1-(v/c)^2}}$ the relativistic *Lorentz-factor*. Using the mass and charge of an electron we get

$$\nu_{\text{syn}} \approx 4.2 \cdot 10^6 \gamma^2 \left(\frac{\text{B}}{\text{Gauss}} \right) \text{Hz} \quad (1.6)$$

As a result, in order to reach frequencies in the X-ray domain, we need electrons at highly relativistic speeds ($\gamma > 1000$) and strong magnetic fields in the area of 10^6 G.

Cyclotron Radiation

For magnetic field strengths on the order of 10^{12} G (Kreykenbohm, 2004), the description of radiation generated by moved particles cannot be accomplished with the theory of synchrotron radiation anymore. Instead, quantum mechanical effects lead to the circumstance, that charged particles can no longer move along arbitrary trajectories perpendicular to the magnetic field lines. Instead they can only follow trajectories of quantized energies, which are called *Landau-levels*. Using n as a quantum number, their energies can be calculated by

$$E_n = mc^2 \sqrt{1 + \left(\frac{p_z}{mc} \right)^2 + 2n \frac{B}{B_c}} \quad (1.7)$$

where p_z is the momentum of the particle parallel to the magnetic field lines (in z-direction) and B_c a critical magnetic field strength. $n = (2j + l + 1)$ is the general quantum number, j the angular momentum and l the spin quantum number. The critical magnetic field strength is given by

$$B_c = \frac{m^2 c^3}{eh} \quad (1.8)$$

For fields stronger than the critical field, relativistic corrections become necessary to correctly depict the energies of the Landau-levels. In highly magnetized plasmas, transitions between these levels can be triggered by high-energy photons, which will cause the spectrum to show characteristic cyclotron absorption lines in the resulting stellar spectrum.

Comptonization

One way for photons to interact with matter is the process of *Compton*¹⁶-*scattering* (refer to Figure 1.5). An incoming photon will transfer part of its energy onto a free electron, changing both their momentum and thus the kinetic energy of the electron. In a non-relativistic case, this energy transfer from photon to electron is described by

$$E_{\text{final}} = \frac{E_{\text{initial}}}{1 + (E/m_e c^2)(1 - \cos \theta)} \quad (1.9)$$

where E_{final} is the final energy of the photon after the interaction, $E_{\text{initial}} = h\nu$ the initial energy of the photon, m_e the mass of the electron and θ the scattering angle. The effects of this process can be observed in surroundings, where the energy of the photons exceeds the energy of the electrons. In hot plasmas however, the opposite situation can occur. In this case, electrons can have a kinetic energy which is higher than the energy of the surrounding photons (usual limit approx. $4k_B T_e > E_{\text{photon}}$). In an interaction between electron and photon, it is now possible for the electron to transfer part of its kinetic energy onto the photon, thus shifting it to shorter wavelengths. This process is called *inverse Compton-scattering*. If this interaction takes place multiple times before a photon can escape the plasma, it can be shifted up to keV energies, which is called *comptonization*. During this process, photons are accumulating energy from the surrounding gas particles and are therefore effectively cooling the plasma. A spectrum which is characterized by comptonization can also be described with a power-law and shows the typical exponential cut-off.

Nuclear Processes

Lastly, nuclear processes can be a source for the production of high energy X-ray photons as well. Contrary to the other cases, highly energetic photons, originating from an atomic nucleus, are denoted with the subscript γ , to distinguish them from photons originating from electronic transitions. Just like electrons, protons have energy levels, that correspond to a shell-like structure and can obtain configurations which are energetically favorable or unfavorable. After a nuclear reaction, such as fusion or fission processes, the atomic nucleus can be in an excited state, which is energetically unfavorable and unstable. The nucleus can get rid of the excess energy by sending out a high-energy photon.

¹⁶Arthur Holly Compton (*1892, †1962) was a US physicist and recipient of the Nobel Prize for physics in 1927.

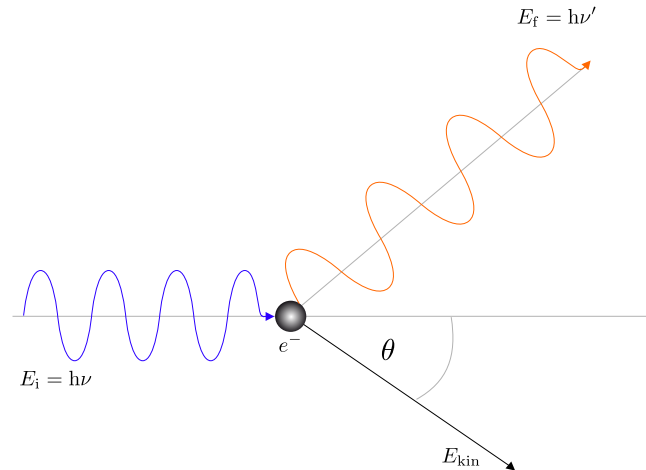
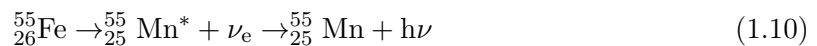


Figure 1.5: Illustration of a Compton-scattering process. The incoming photon transfers part of its energy onto the electron. Its wavelength is red-shifted, due to the loss of energy. The electron on the other hand has gained kinetic energy and is scattered under an angle θ .

Also, the *inverse β -decay* can cause the emission of an X-ray photon. In this case, an atom's nucleus can capture an electron from the surrounding K-shell, creating a neutron and a electron-neutrino, leaving behind a vacant state in the K-shell. According to the previously described processes, this vacant state can be filled with either a free electron or one from a higher energy shell, creating an X-ray photon in the transition.

One very important nuclear process for high energy astrophysics, is the radioactive decay of Fe-55, which is also commonly used in laboratory test-setups for calibration measurements of high-energy photon detectors, such as *Charge-Coupled Devices* (CCDs) oder *Depleted P-type Field-Effect Transistors* (DEPFETs). The reaction equation



describes this process, where the asterisk in ${}_{25}^{55}\text{Mn}^*$ denotes, that the nucleus is in an excited state and can only change into a more stable configuration by emitting a photon. This mechanism produces two very distinct K-series lines (K_α and K_β) which can be found at energies of 5.9 keV and 6.49 keV respectively.

1.4 Physical Processes of X-ray Interaction with Matter

There are several ways for photons to interact with matter, which become dominant for certain photon energies and certain atomic numbers Z of the target material (refer to Figure 1.6). The most important processes will be described in the following section. Roughly, they can be split into three mechanisms:

photoelectric-effect	dominant for $E_{\text{photon}} < 50 \text{ keV}$
Compton-scattering	dominant for $60 \text{ keV} < E_{\text{photon}} < 10 \text{ MeV}$
pair-production	dominant for $E_{\text{photon}} > 10 \text{ MeV}$

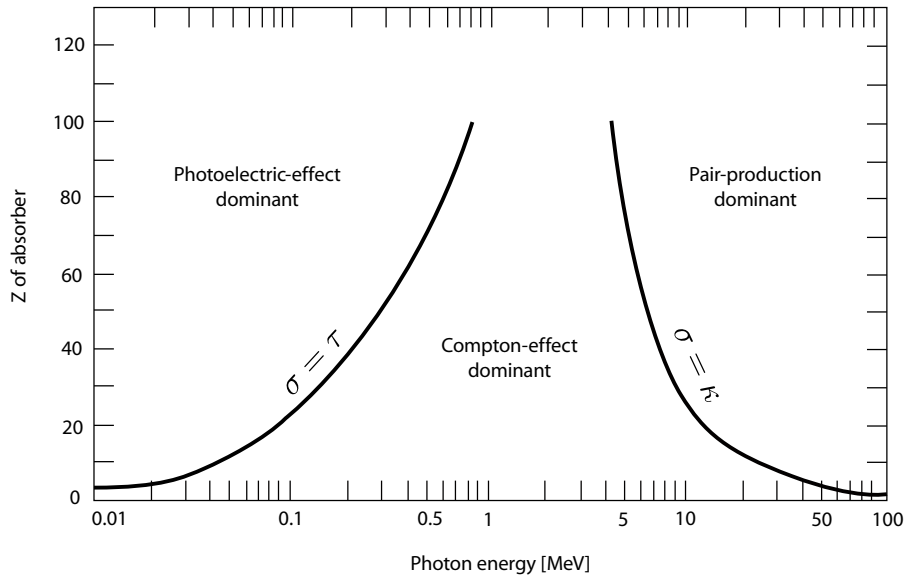


Figure 1.6: The plot shows the importance of the three main X-ray interaction processes and their dependence on the photon energy (x-axis) and atomic number Z of the target material (y-axis). There are three distinct areas in which either the photoelectric effect, Compton-scattering or pair-production are the dominant interaction mechanisms. (Evans, 1955)

All of these three cases have in common, that they are single event processes, which means, that a photon is absorbed or scattered in one single event and not in a series of multiple events or cascades. Also, energy and momentum of the incoming photon are completely or partially redistributed to other involved particles in each process.

In general, the *Beer¹⁷-Lambert¹⁸ law* for photon absorption describes the change of intensity I of a photon beam with the penetration depth x into a material which is characterized by the absorption coefficient μ .

$$I(x) = I(0) \cdot \exp(-\mu x) \quad (1.11)$$

The expression $I(0)$ denotes the initial intensity of the photon beam, which can be seen as a measure for the number of photons per beam-volume. The absorption coefficient μ is dependent of the material and the photon energy and results from the summed up cross-sections of each individual process, as well as the density and mass of the interacting matter. This exponential relationship between intensity and penetration depth is typical for uncharged particles and stands in contrast to the interaction of charged particles with matter, which are cascades of single events. They can be described with the Bethe-Bloch formula. (Bille and Schlegel, 2002)

¹⁷August Beer (*1825, †1863) was a German mathematician, chemist and physicist.

¹⁸Johann Heinrich Lambert (*1728, †1777) was a Swiss mathematician and physicist.

1.4.1 The Photoelectric-Effect

The *photoelectric-effect* is one of the major three microscopic effects, which can explain the interaction of photons with matter. The energy of the photon E_{photon} is hereby completely used to remove an electron with binding energy E_{B} (< 0 eV) from the atom. If the energy of the photon is greater than the absolute value of E_{B} , the rest of the energy is transformed into kinetic energy E_{kin} of the electron, satisfying the equation

$$E_{\text{photon}} = E_{\text{kin}} - E_{\text{B}} \quad (1.12)$$

The ejected electron will leave behind a vacant state within the electron shell of the atom, which can be occupied by electrons from higher energy states. This transition from higher to lower energies releases energy in form of a fluorescence photon or via *Auger*¹⁹-*electrons*.

1.4.2 Compton-Scattering

In the context of X-ray creation, the process of Compton-scattering was already discussed briefly in Section 1.3.2. In both hot and cool gases, X-ray photons can transfer part of their energy onto bound or free electrons. For the energy range in which Compton-scattering is the dominant interaction mechanism, binding energies in an atom can be neglected and electrons can be considered as free particles. During the interaction, part of the incoming photon energy is transformed into kinetic energy of the electron, causing the photon's wavelength to increase. The efficiency of this process is strongly dependent on the scattering angle between photon and electron and the relation between initial and final wavelength of the photon can be described with the expression

$$\Delta\lambda = \lambda_{\text{final}} - \lambda_{\text{initial}} = \frac{h}{m_e c} \cdot (1 - \cos\theta) \quad (1.13)$$

For $\theta = 0$ we get the same incoming and outgoing wavelength, which means, that the photon passed the electron without any interaction. For an angle of $\theta = \pi$ the right hand side of the equation is maximized, meaning that the photon was reflected from the electron and a maximum amount of energy was transferred in the interaction. Statistically, the distribution of occurring scattering angles can be calculated using the differential cross-section by Klein²⁰-Nishina²¹ (Bille and Schlegel, 2002). For photon energies around 10 keV almost all energy remains with the scattered photon whereas for higher energies around 10 MeV almost all energy is transferred to the scattered electron, therefore effectively heating up the gas.

1.4.3 Pair-Production

Pair-production is the most exotic process of the three main interaction processes and can only take place at photon energies of $E_{\text{photon}} = 1.022$ MeV or higher. The reason for this is, that an electron-positron pair will be created spontaneously and that the initial energy of the photon will have to be equal or higher than the rest mass ($= 511$ keV) of the two resulting particles. Pair-production is only possible in the vicinity of an atomic nuclei, making this

¹⁹Pierre Victor Auger (*1899, †1993) was a French physicist.

²⁰Oskar Benjamin Klein (*1894, †1977) was a Swedish theoretical physicist.

²¹Yoshio Nishina (*1890, †1951) was a Japanese physicist and is commonly considered the founding father of modern physics research in Japan.

process an interaction process with matter. The reason for this comes from particle physics and is due to the fact, that the emission-angle between the two particles is 180° . Hence, their resulting total momentum will equal zero and violate momentum conservation principle for the photon. Instead, the momentum will be transferred to the nucleus in the vicinity of the creation vortex, satisfying momentum conservation for all involved particles.

1.5 Astrophysical X-ray Sources

After the discoveries of Uhuru, it became obvious, that there were more astronomical sources emitting X-rays than previously assumed. Missions like OSO-7²² and ROSAT were launched to survey the sky and helped to map and classify many of these sources. Today, astrophysicists mainly distinguish between galactic and extra-galactical sources, some of which will be presented in the following paragraphs. It has to be noted however, that it is not possible to cover all known types of sources in the scope of this thesis. The number of variations within these object classes is constantly increasing, making it more practical to focus on the main types, which can be considered representatives of their corresponding groups.

1.5.1 Galactical Sources of X-ray Radiation

Stars

Stars are by far the most common source of X-rays in the universe, since they outnumber any other type of X-ray emitting object by orders of magnitudes. Due to its proximity to us, the Sun is the brightest source of X-rays in the sky. Most of the time however, the surface temperature of most stars is too low for X-rays to dominate the blackbody spectrum and stars like the Sun (spectral type G2) only emit a small portion of 10^{-6} of their luminosity in the X-ray band. The source of these photons is the stellar corona, which has a temperature of a few million degrees for our Sun and is hot enough to explain emission via blackbody radiation. The exact reason for such high coronal temperatures is currently unknown, especially since the surface temperature of typical stars is just on the order of $10^3 - 10^6$ K. It is believed however, that plasma ejections from flaring events on the stellar surface can inject enough energy into the coronal material to heat it up considerably. These flaring events are usually located near *sunspot regions*, which depict regions of complex magnetic field structures and where magnetic field lines can reach all the way from the stellar surface into the stellar corona. These field lines are usually grouped together in tubes (so-called *coronal loops*) and can store chunks of plasma in between (an example of such loops on the surface of the Sun can be seen in Figure 1.7). Due to the differential rotation of most stellar objects, these configurations are not stationary and get more and more twisted until a point of instability is reached. A process called *magnetic reconnection* describes a scenario of snapping field lines, which almost instantaneously reconnect into more stable configurations, ejecting the trapped plasma from the star's surface into the interstellar medium while at the same time, heating up the gas masses around it in the stellar corona. These incidents are called *stellar flares* and are among the most energetic events that occur in main-sequence stars (Qiu, 2007).

²²Orbiting Solar Observatory mission 7, part of a series of X-ray missions. It was primarily a solar observatory designed to point a battery of UV and X-ray telescopes at the sun. NASA/HEASARC

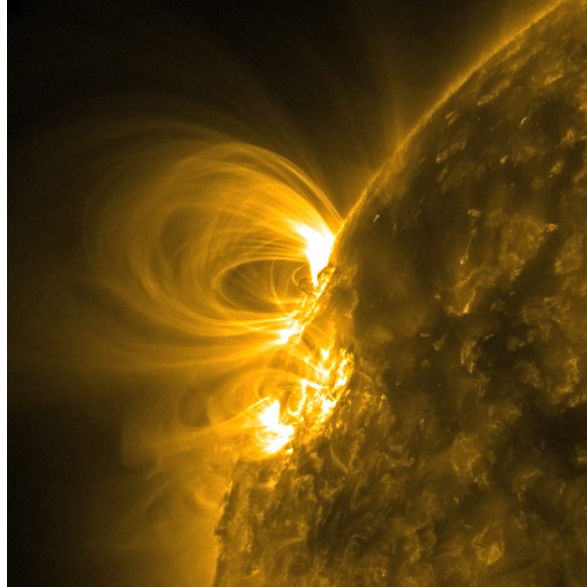


Figure 1.7: Hot plasma is trapped in between magnetic field lines that form so-called coronal-loops. Image recorded by NASA's *Solar Dynamics Observatory* (SDO) in 2011. Photo was taken in extreme UV band. NASA/SDO

Supernova Remnants

Supernovae are the most energetic and violent events in the Universe, which disrupt whole stars while emitting large amounts of energy and particles at relativistic speeds into the surrounding medium. They are classified into many different categories, which are characterized by their light-curves, involved chemical elements of the progenitor stars and physical processes causing the explosion. One thing, that all these different types have in common though, is the explosive release of vast amounts of energy ($\sim 10^{51}$ erg/s) within a timeframe of a few seconds at the end of a star's life. This energy causes single stars to have a luminosities ($\sim 10^9 L_{\text{sun}}$), that can even outshine whole galaxies before fading away and leaving behind much less-luminous *compact objects* (COs) (see Figure 1.8). The ejecta of a supernova (hull-material, which surrounded the stellar core prior to the explosion) can reach velocities up to 10^3 km/s, generating *shock-fronts* traveling through the still in-falling hull-material from outer regions of the star. They can create expanded structures of gas, which cool down and remain visible as so-called Supernova Remnants, which are visible throughout the whole electromagnetic spectrum.

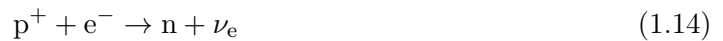
Pulsars

After the explosion of very massive stars ($M_* \gtrsim 8 M_{\text{sun}}$) a compact object remains within the ejecta of the Supernova. The class of this CO is determined by the final mass of the stellar core and can either be a *Neutron Star* (NS) or a *Black Hole* (BH). For core masses



Figure 1.8: Hubble image of Supernova SN1994D at the edge of its host galaxy NGC4526. The luminosity of the Supernova in the lower left corner is comparable to the luminosity of the entire galaxy, even though just one single star is involved in the process. NASA/HST

in between the Chandrasekhar mass $M_{\text{Ch}} = 1.44 M_{\text{sun}}$ and the *Tolman²³-Oppenheimer²⁴-Volkoff²⁵ limit* of $M_{\text{OV}} = 3 M_{\text{sun}}$ the internal gas pressure becomes high enough to support the inverse beta-decay of the protons.



Since the object is now mainly composed of neutrons it is called a neutron star, having a mass of around 1-3 M_{sun} and a radius of approximately 10 km. Large portions of the initial angular momentum of the star are conserved during the collapse, causing a NS to have an increased spin-velocity by many orders of magnitude. As a result, NS are rapidly rotating objects, with periods of milliseconds for some of them. Furthermore, most of the initial magnetic flux is conserved, causing Neutron Stars to have very strong magnetic fields, which also spin within the ionized gas masses surrounding them. A rotating magnetic field will induce a strong electrical field setting surrounding electrons into helical motion around the field lines (as described in 1.3.2). As a result, synchrotron radiation is emitted from cones along the magnetic axis. If this axis is not parallel to the spin axis of the NS, the emission cones will rotate around it, creating a *lighthouse effect* for every object located within their line-of-sight. If Earth is located within such a lighthouse beam, pulsed radiation can be measured, justifying the name *pulsar* for these kinds of objects. One of the most important pulsars in

²³Richard Chace Tolman (*1881, †1948) was an American mathematical physicist and physical chemist. He is best known for his contributions to statistical mechanics.

²⁴Julius Robert Oppenheimer (*1904, †1967) was a US theoretical physicist and professor of physics at the University of California, Berkeley. He is best known for his role in the development of the first atomic bomb.

²⁵George Michael Volkoff (*1914, †2000) was a Canadian physicist, who is most-commonly known for his prediction of the existence of neutron stars together with J. Robert Oppenheimer.



Figure 1.9: At the center of the Crab nebula, a pulsar rotates with a spin period of only 33 ms (image is a combination of optical and X-ray observations). NASA/CXC/SAO

X-ray astronomy is the *Crab pulsar* (PSR B0531+21), which has a rotation period of just 33 ms (Tavani, 2011) (see Figure 1.9).

X-ray Binaries

In general, a stellar binary system consists of two gravitationally interacting stars, which orbit around a common *center of mass* (CM). For *X-ray binaries*, the system must consist of a regular main-sequence star or *red giant* and a compact object emitting X-rays (as defined in Section 1.5.1). Depending on the mass of the regular star, such systems are called *Low Mass X-ray Binaries* (LMXB, for $M \approx 1 M_{\text{sun}}$) or *High Mass X-ray Binaries* (HMXB, for $M > 10 M_{\text{sun}}$). In such a system, gas masses can be transferred from the regular companion (called the *donor*) onto the compact object (called the *acceptor*). This material however, cannot fall directly onto the surface of the CO, but has to dissipate its angular momentum first, thus often forming an *accretion disk* surrounding the CO (refer to Figure 1.10). The mechanism of *accretion* is one of the most efficient energy transformation processes in the universe and will transform gravitational potential energy of the gas masses into radiation. Consequently, accretion disks are very hot and can reach temperatures of a few million degrees, emitting thermal blackbody spectra peaking in the X-ray band. Depending on the configuration of the binary system, astrophysicists distinguish between three different accretion mechanisms.

Roche-Lobe-Overflow By definition, the *Roche-lobe* of a star is a region around its volume in which matter is gravitationally bound to the star. If matter can escape the Roche-volume it can also escape the star's gravitational pull. In a binary system, there are two massive bodies exerting a gravitational pull on any material present in their common vicinity. The Roche-lobe of each star is therefore deformed into a teardrop shape (see Figure 1.11). If one of the stars grows beyond its Roche-volume, matter will enter the Roche-lobe of the companion



Figure 1.10: Artist's impression of an X-ray binary system. Mass from the donor star forms an accretion disk around the acceptor. The hot disk emits photons peaking in the X-ray band of light. Image by Mark A. Garlick / space-art.co.uk

star, thus "falling" onto its surface. This process is called *Roche-lobe overflow* and represents a very effective way for accretion to occur in binary systems. As pointed out in the previous paragraph, this material cannot fall directly onto the acceptor, but has to dissipate its angular momentum first. It will gather in an accretion disk around the star, which is constantly heated up by in-falling particles (up to 10^7 K), turning potential into kinetic energy and finally into radiation via blackbody emission.

If the accreting object is a NS, most of the X-ray radiation will be emitted via the bremsstrahlung mechanism, when in-falling charged particles from the donor star reach the hard surface of the NS and are slowed down abruptly.

Wind-Accretion If the donor star is an early type star of spectral type O or B, the process of *wind-accretion* can occur. Such stars generate strong stellar winds, since radiation, which is generated in the interior of the star, cannot escape through the opaque material of the star's surface. Such stars are close to the *Eddington*²⁶ *limit* where the gravitational force is equaled by the force due to radiation pressure from photons originating from within. Once the *Eddington luminosity* is exceeded, the force due to radiation pressure will overcome the gravitational pull and eject matter from the stellar surface together with the escaping photons. Typical loss ratios are between 10^{-10} to $10^{-5} M_{\text{sun}}$ per year. Mass, which is transported to the acceptor via this mechanism, only carries small angular momentum (due to high radial velocities) and will therefore only form a small accretion disk, compared to the process of Roche-lobe overflow. This process is also called *Bondi*²⁷-*Hoyle*²⁸ *accretion* and plays a

²⁶Sir Arthur Stanley Eddington (*1882, †1944) was a British astrophysicist.

²⁷Sir Hermann Bondi (*1919, †2005) was an Anglo-Austrian mathematician and cosmologist. He is best known for his development of the steady state theory of the Universe.

²⁸Sir Fred Hoyle (*1915, †2001) was an English astronomer and mathematician. He is known primarily for his contribution to the theory of stellar nucleosynthesis.

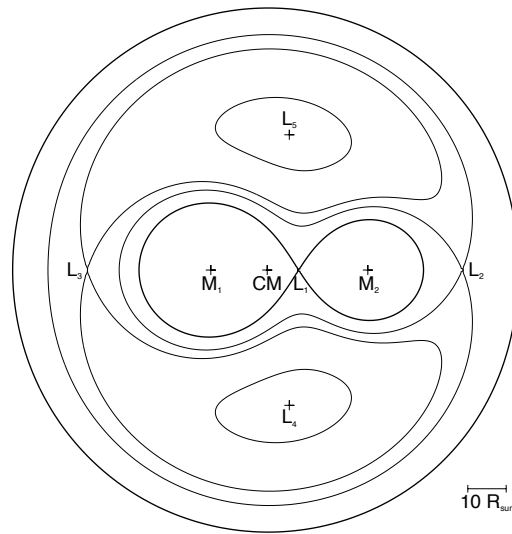


Figure 1.11: The image shows lines of equal potential for the two body problem with masses $M_2 < M_1$. The innermost lines define the Roche-lobes of the two involved masses. CM denotes the center of mass of both objects and L_n so-called Lagrangian points, which are force-free points of the two-body problem. These points will also play an important role in the IXO mission, since IXO will be placed in an orbit around Lagrangian point L_2 of Earth and Sun. Image from (Wilms, 1996)

dominant role for HMXBs.

Be-Stars If the companion of the donor star is a so-called Be-star, a third variation of accretion occurs. Be-stars have small rotation periods and experience strong centrifugal forces, which cause them to deviate from a spherical shape. They can develop disk-like bulges around their equatorial regions, which can touch the compact companion's surface during an orbit and accrete matter onto them. If this happens, X-rays are produced just as explained above. Astrophysicists distinguish between two types of these systems. If the donor's bulge touches the companion at all times during the orbital period, the system is called *persistent*. If they only touch for part of the orbital period, they are called *transients* and will not emit X-rays all the time, but in periodic *bursts*. In general, the terms transient and persistent are used to describe systems, which emit radiation constantly or temporarily.

1.5.2 Extragalactic Sources of X-ray Radiation

Active Galactic Nuclei

Active galactic nuclei are amongst the most massive and farthest objects we can observe in the universe. They represent the core regions of very massive galaxies showing strong electromagnetic emission throughout the whole spectrum or in certain distinct energy bands. Even though AGN come in a large variety of types, Urry and Padovani (1995) suggested one common structure for all of them and explain their difference in appearance by effects, which are due to different viewing angles from Earth. The center of such an object is supposed to

contain a *Supermassive Black Hole* (SMBH), with a mass of 10^6 up to $10^{10} M_{\text{sun}}$ and around which a large accretion disk has formed. The source region is furthermore surrounded by a thick dust torus and several gas-clouds, which orbit at different velocities. Sometimes AGN can have extended, highly-relativistic outflows of hot plasma, originating from their polar regions, which can extend far into the *Intergalactic Medium* (IGM) and are sources of *radio-synchrotron radiation*. These *jets* are perpendicular to the galactic disk and their exact nature and cause is topic of current scientific investigations.

Clusters of Galaxies

Just as stars can gather in large groups, which are called galaxies, also galaxies can gather in large gravitational groups, called clusters of galaxies. Such groups usually contain a few up to tens of thousands of galaxies and are the largest structures in the Universe known to mankind. The huge gravitational potential of these systems also traps a lot of gas, called the *Intercluster Medium* (ICM). This gas has very high temperatures of around $10^7 - 10^8$ K (Unsoeld and Baschek, 2005) and can emit X-ray radiation via bremsstrahlung and blackbody emission. From their luminosity in X-rays and optical light, astrophysicists are able to derive the mass contained within these clusters. They can therefore serve as "laboratories" for the probation of theories connected to dark matter research and are very important cosmological indicators.

Many of the objects described on the previous pages will be investigated by IXO throughout the electromagnetic spectrum of 0.5 - 40 keV. In order to gather as much information as possible about their physical processes and environments, a variety of detectors and instruments will be used. One of them will be the Wide-Field Imager, which is the most important instrument for this thesis and will be a Silicon-based pixelated photon detector. In order to lay the groundwork for a detailed understanding of this instrument, the next chapter will focus on the basic physics of semiconductors and the characteristics, obstacles and possible applications, which arise from them.

2 Semiconductor Detectors

The most important requirements of modern day astronomical photon detectors are high collection efficiencies and *energy resolutions*. Both aspects are fulfilled by semiconductor based detectors, which have become the main detector type for countless optical and X-ray astronomical missions in the past decades. Especially in the field of X-ray astronomy, where incoming photons in the range of 0.1 - 20 keV generate hundreds or thousands of electron-hole pairs in the semiconducting material, their QE and SNR are important assets when observing dim sources at large distances. Additionally, with the advances of digital photography in the private sector, manufacturing processes for semiconductors have been refined and brought down in cost considerably in the last years.

Before diving deeper into this rapidly evolving technological field, a short introduction to semiconductors and their relevant physics will be given in Section 2.1, which is mainly based on Turton (2000). Furthermore, Section 2.1.2 is based on Spieler (2005), while Sections 2.4 and 2.4.3 were written with information from Martin (2009).

2.1 Basic Physics of Semiconductors

On the microscopic level of solids, electrons can no longer be characterized by their location and momentum, but by their corresponding quantum mechanical wave-function. In the periodic lattice of a solid, where atomic nuclei are arranged in regular patterns at fixed distances, the wave-functions describing electrons in the atomic shells can overlap and the affiliation to their corresponding atomic nuclei is lost. Consequently, the discrete energy levels of individual atoms will smear out into *energy bands* of allowed and forbidden energies¹ for any electron within the solid. This situation can be explained as follows: For two spatially separated atoms, there is no interaction between their electrons, which occupy certain discrete energy levels. As these two atoms are moved closer together, their electrons will begin to interact and the combined system of atoms will have altered electronic energy states. For two sodium atoms for example, two discrete 3s energy levels would be created for the corresponding valence electrons, one with a higher and one with a lower energy. For a system of N atoms, N discrete energy levels will be created respectively, thus partitioning an energy range of a few eV into N discrete energy levels. For solids, the number N of atoms within the lattice is usually on the order of 10^{24} , rendering gaps between these discrete energy levels practically negligible. Consequently, within an energy band, energy levels form a *near-continuum*, which will be filled with electrons, starting with the lowest available energy. In case of sodium, this will result in fully occupied 1s, 2s and 2p bands, but only a partially filled 3s band (we can have $2N$ electrons in N states of the 1s band for example, but for the $2N$ available states in the 3s band, there are only N valence electrons to occupy these states). The highest energy an

¹These allowed and forbidden energies are a consequence of the solution of the Schrodinger equation for the periodic potential of the solid-state lattice.

electron will have in such a configuration at a temperature of 0 K is called the *Fermi²-energy* E_F and plays an important role in solid-state physics. The probability $f(E)$ of occupancy of electronic states of energy E is described with the *Fermi-Dirac³ distribution*

$$f(E) = \frac{1}{\exp\left(\frac{E-E_F}{k_B T}\right) + 1} \quad (2.1)$$

and is equal to 1 for all energies E below the Fermi-Energy E_F (see Figure 2.1). As mentioned earlier, the valence electrons of the atoms, that make the solid, are located within a partially or completely filled energy band, which is called the *valence band*. Also a higher energetic band will form due to the electronic interaction of this configuration, which is called the *conduction band*. As the name suggests, electrons which are located in the conduction band can contribute to the electronic conductivity of a certain solid, while electrons in the valence band cannot (if the band is completely filled). Vacant energy states in the valence band, which result if electrons change into the conduction band, are called *holes* and contribute to the conductivity of a solid. Formally, these holes can be treated as free positive charges. The distance in energy between the valence and the conduction band is called the *band-gap* and is denoted with the symbol E_g . It is mainly dependent on the lattice structure and represents a very important characteristic of the solid. According to the size of this band-gap, solids are distributed into three main groups (assuming a temperature of $T = 0$ K - refer to Figure 2.2).

Isolators For isolators, the valence band and the conduction band are far apart, thus resulting in a large band-gap. Typically, values of $E_g > 3$ eV are characteristic. Such band-gaps cannot easily be overcome by thermal excitation, since $k_B T$ is about 0.025 eV for room temperature (≈ 300 K). Moreover, the valence band of isolators is fully occupied, thus offering no available energy states for electrons to participate in the conduction process. Consequently, these solids do not conduct electricity, even at very high temperatures.

Metals Metals only have a partially filled valence band, meaning, that within the valence band, there are still available energy levels for electrons, which can easily be thermally excited. In that case, electrons can participate in the conduction process, thus making metals conductive at very low temperatures already. In order to unify this circumstance with the model of valence and conduction bands, metals are said to have overlapping valence and conduction bands, resulting in a non-existent band gap.

Semiconductors Semiconductors are the most interesting class of solids, since they can behave as both - conductors and isolators - depending on their temperature. Just like isolators, they have completely filled valence bands, making it impossible to conduct electricity at $T = 0$ K. Their band-gap however is fairly small with values of $0 \text{ eV} < E_g < 3 \text{ eV}$ and can be overcome by thermal excitation. For temperatures, that correspond to thermal energies below

²Enrico Fermi (*1901, †1954) was an Italian physicist and recipient of the Nobel Prize for physics in 1938. He is best known for his contributions to quantum theory, nuclear and particle physics and statistical mechanics.

³Paul Adrien Maurice Dirac (*1902, †1984) was an English theoretical physicist and recipient of the Nobel prize for physics in 1933. He is best known for his major contributions to quantum mechanics.

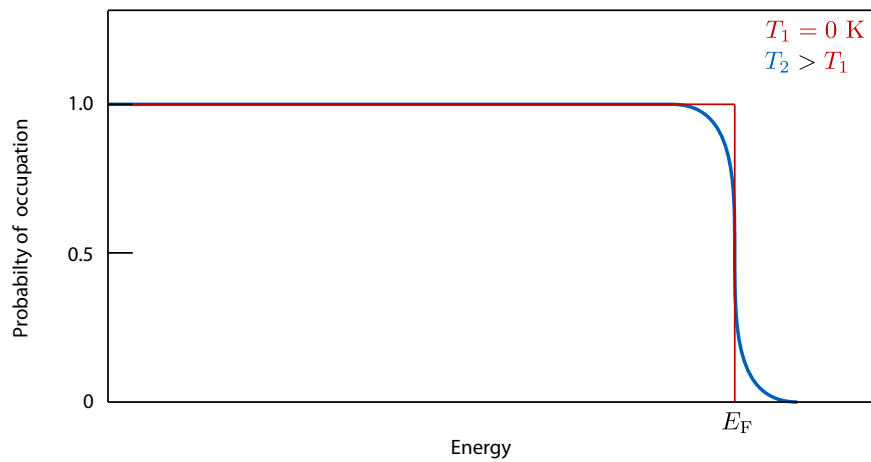


Figure 2.1: The Fermi-Dirac energy distribution. The graph shows the probability of occupation of an electronic state with energy E . At $T = 0$ K, all energy levels up to a highest energy, the so-called Fermi-energy are occupied. For $T > 0$ K, electrons will also occupy higher energy states, thus reducing the probability of occupation for states just below the Fermi-energy.

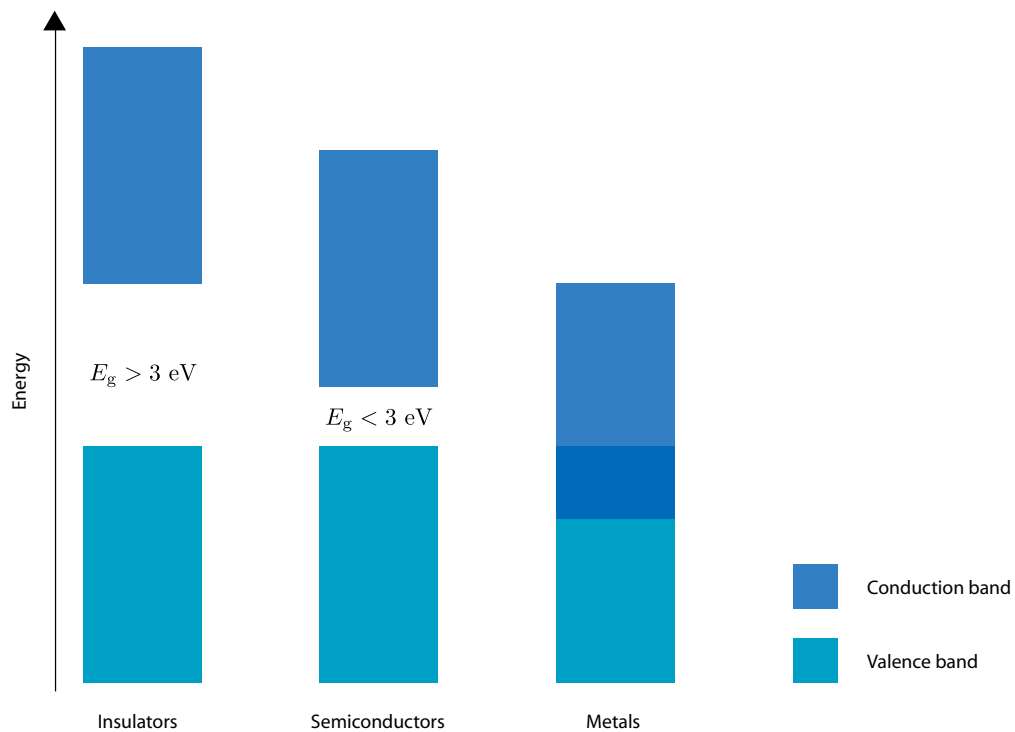


Figure 2.2: Schematic representation of the three main groups of solids, depending on the size of their corresponding band-gap.

Table 2.1: Table of common detector materials and their corresponding band-gap and electron-hole pair energies in eV, as well as their dielectric and atomic numbers ϵ and Z respectively. (Spieler, 2005)

Material	E_g [eV]	E_{eh} [eV]	ϵ	Z
Silicon (Si)	1.12	3.6	11.7	14
Germanium (Ge)	0.67	2.96	16	32
Gallium Arsenide (GaAs)	1.43	4.2	12.8	31.5
Diamond	5.5	13	5.7	6
Indium Phosphide (InP)	1.35	4.2	12.4	32
Cadmium Telluride (CdTe)	1.44	4.43	10.9	50

the band-gap, the solid will behave like an isolator, whereas for energies above the band-gap, it will act as a conductor. Table 2.1 gives an overview over a few important detector materials and their corresponding band-gaps. It is important to note, that the energy needed to create an electron hole pair is usually larger than the corresponding band-gap of the material. The reason for this is, that both bands have a finite energetic width, so that transitions between valence and conduction bands are not sharp. Furthermore, energy which is transferred onto the solid, is also used to create *phonons*, which are lattice vibrations of the atomic nuclei. Taking all these physical processes into account, the mean energy E_{eh} to create an electron hole pair in Germanium for example is 2.96 eV while its band-gap energy is only at $E_g = 0.67$ eV.

2.1.1 Doping of Semiconductors

So far, all the explained characteristics of semiconductors were true for so-called *intrinsic* or extremely pure semiconductors. Additional to the characteristics above, the conductivity of a semiconductor can be actively altered by a process called *doping*. When doping a semiconductor, substitute atoms (or *impurities*) - which have one electron more or less than the atom they replace - are deliberately introduced into the material in small concentrations (usually in parts per million amounts). Depending on whether the dopant material has more or less electrons than the semiconductor material, they are called *n-type* (n = negative, increasing the number of negatively charged carriers) or *p-type* (p = positive, increasing the number of positively charged carriers) semiconductors. Taking Silicon (Si) as an example, all valence electrons are used to form covalent bonds of the Si-atoms. By introducing a Phosphorus (P) atom however, only four valence electrons are used for the covalent bond, while the fifth electron (called the *donor*) remains almost free, since it does not participate in the bonding process. This electron is weakly bound to its P-atom and only needs a small energy transfer to change into the conduction band.

In case of a p-type semiconductor, a vacant state, which is called an *acceptor state* remains where a covalent bond should be. Electrons from the valence band of the semiconductor can fill these acceptor states and create holes in the valence band, which can be used to conduct electricity.

In the picture of energy bands, donor states are located just below the conduction band, while acceptor states are located just barely above the valence band, thus making small thermal

excitations sufficient to allow conductivity in the doped material. In combination n-type and p-type semiconductors have interesting characteristics, which can be exploited for the efficient detection of electromagnetic radiation and will be explained in the following paragraph.

The pn-Junction

One of the most important geometries in semiconductor physics is the *pn-junction*, which is created by bringing together a p- and n-type semiconductor in thermal equilibrium. Relative to each other, a large difference in the concentration of their majority carriers exists, causing the electrons for the n-type and holes for the p-type areas to diffuse into the other material, where they will recombine with present electrons or holes. As a result, the number of carriers in the vicinity of this contact region is substantially reduced, forming a so-called *depletion region*, that does not contain any mobile charge carriers anymore. While the movement of charge carriers (current $I_{\text{diffusion}}$) into the other material is going on, it will increase the size of the depletion layer and leave uncompensated charges behind in the source area. Consequently, an electrical field (so-called *contact potential*), which is oriented from the n-type to the p-type region will emerge. Thermally created electrons in the conduction band of the p-type material will now be attracted to the n-type side of the junction and will create a current I_{drift} , which is directed into the opposite direction of $I_{\text{diffusion}}$ and due to the electric field across the junction. Once an equilibrium state is established, this drift current I_{drift} will be constant and just as large as the diffusion current $I_{\text{diffusion}}$ of the contact (see Figure 2.3a).

An interesting scenario occurs, if an external voltage is applied to the pn-junction. If a negative voltage is applied to the n-type side and a positive voltage to the p-type side, the intrinsic contact potential will be reduced, thus making it easier for conduction electrons from the n-type side to diffuse across the junction and therefore increasing the diffusion current $I_{\text{diffusion}}$. Due to the large amount of available conduction electrons in the n-type material, this current can become quite large if the external voltage is increased. The drift current will remain untouched by this scenario and will not change for this polarization. As a result, $I_{\text{diffusion}}$ will be much larger than I_{drift} , resulting in a net current across the junction from the n- to p-type side. This configuration is also called *forward biasing* of the pn-junction (see Figure 2.3b).

If the polarization of the external voltage is changed (*reverse-biasing*), the contact potential across the junction is furthermore increased, making it less likely for charges from the n-type side to diffuse across the junction into the p-type side. The net current across the junction is then almost solely due to I_{drift} and therefore dependent on the number of thermally created electrons (see Figure 2.3c).

A pn-junction can therefore act as a *gate* that only opens into one direction, but remains closed in the other one. In the field of electronics the pn-junction is called a *diode*.

2.1.2 Using Diodes for Radiation Detection

Diodes fulfill manifold tasks in modern day electronics and are also used for the detection of photons. As already mentioned in Section 2.1.1 the depletion layer is void of mobile carriers and located in between a positively charged n-type and a negatively charged p-type layer. Consequently, this geometry is similar to a capacitor with a dielectric medium in between its plates and can act as an ionization chamber. Charges, which are created in this dielectric,

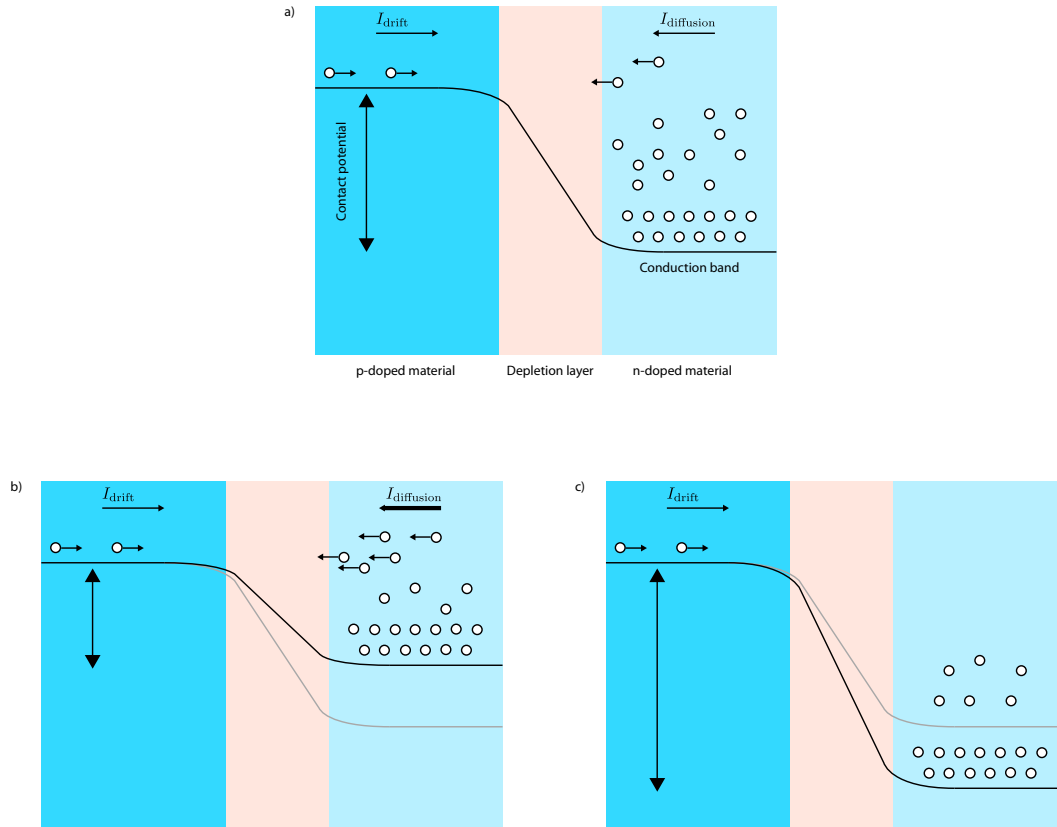


Figure 2.3: (a) Schematic representation of a pn-junction and the contact potential between the p- and n-type layers. The bright area in the center is called the depletion region and is void of mobile charged carriers. Two currents I_{drift} and $I_{diffusion}$ arise from this configuration and will compensate each other as long as no external voltage is applied. (b) A forward biasing voltage is applied between the two n- and p-type layers, causing the potential barrier of the contact potential to be reduced. It is now possible for more carriers to diffuse from the n- into the p-type region, thus increasing $I_{diffusion}$ while I_{drift} remains constant. (c) A reverse biasing voltage is applied to the junction, thus increasing the potential barrier of the contact potential. As a consequence, $I_{diffusion}$ will drop to almost zero, while I_{drift} still remains constant and will now account for a small net flow of charges from the p- to the n-type side of the junction. (Turton, 2000)

will be transported to the respective electrodes and can be measured. For a classical diode however, this depletion region is only of the order of several μm . The application of a reverse-bias voltage can widen the depletion layer, increasing the volume in which charges can be created without recombining with other mobile charges in their vicinity. Spieler (2005) shows, that the width w of the depletion layer is given by

$$w = \sqrt{\frac{2\epsilon V_b}{e} \cdot \frac{N_a + N_d}{N_a N_d}} \quad (2.2)$$

where ϵ is the dielectric constant (11.9 for Si) of the material, V_b the biasing voltage, N_a and N_d the charge carrier densities for acceptors and donors respectively and w the one-dimensional width of the depletion layer in direction perpendicular to the pn-interface. The external biasing voltage V_b and the charge carrier concentrations N_a and N_d are three parameters, that can be technically changed. Increasing the external bias voltage seems like an easy way to increase the width of the depletion zone, but is limited to electric fields $< 10^5 \text{ V/cm}$. Above such fields, electrons can attain enough kinetic energy from the field, in order to create new electron-hole pairs, that would ultimately lead to a destructive avalanche of charged particles within the diode. The second way would be to reduce both the dopant concentrations for the n- and p-type materials, which is ultimately limited to the intrinsic impurities of the crystal itself. It is interesting to note, that charges created in the depletion zone, will not move ballistically towards the p- and n-type side electrodes. Instead, while moving towards the electrodes, they will interact with the crystal itself and transfer part of their kinetic energy from the field onto the lattice, thus creating phonons and heating up the material. As a consequence, their traveling velocity is almost constant and only a function of the electron mobility and the electric field created by the external biasing voltage.

2.1.3 The Concept of Sideways Depletion

The interaction cross-section for photons with a solid state material is strongly dependent on the photon energy (E^{-3} in case of the photoelectric absorption). Optical photons for example will already be absorbed close to the surface of the semiconductor, while X-rays can reach far into its interior, until they are fully absorbed. On their way through the material, they will create a multitude of electron-hole pairs depending on their energy. However, only some of these charges will be created within the depletion zone and not recombine. As mentioned in Section 2.1.2 the depletion layers are usually rather small and only in the range of a few microns. One way to fully deplete the bulk material of a photo diode is by applying the principle of *sideways depletion* to the detector. A typical configuration for sideways depletion is an n-doped silicon wafer, which is sandwiched between two p-type layers on each side. By applying a reverse bias voltage of around 200 V between the n-type bulk and both p-type layers, two separate depletion regions will form and merge in the center of the bulk material. As a result, the bulk will be fully depleted, thus removing any mobile carriers, that could interact with produced electron-hole pairs. Moreover, sideways depletion does not only increase the sensitive area of the photo-diode to the whole bulk material, but it also allows to irradiate the detector from the back, so-called *backside illumination*. The resulting advantage is, that all readout electronics, which have to be located close to the p-type side used for readout, are moved out of the way of incoming radiation and will neither be damaged by their ionizing effect nor alter its flux by absorbing photons, that would have otherwise hit

the detector material. By applying two separate reverse-bias voltages it can be achieved to move the potential minimum of the n-type material from its center close to its surface where the readout electrodes are located, which is a very important aspect for the functionality of a CCD (further explanation in Section 2.2).

2.1.4 Pixelated Photon Detectors

It is known from fundamental optics, that in order to create a real picture of an object, a focussing optic is necessary to create a one to one correlation between a point of the object and a point on the detection screen. Even though focussing highly energetic X-rays is a problem all by itself, Wolter-telescopes can be used instead of refracting lenses or classical reflecting mirrors. The second part of an imaging system - the screen, which will be replaced by a photon detector - needs to be a matrix of multiple points, so that coordinates in the resulting image can be related to coordinates of the recorded object. Consequently, modern day semiconductor photon detectors are mostly divided into so-called *pixels*, which are small photon detectors usually rectangular in shape and combined in a two-dimensional array to mimic a typical screen or photo plate.

A common way of achieving such a segmented substructure is by dividing the electrodes on top of the depleted bulk material of the detector into multiple units. The bulk unit can be a n-type substrate, while the readout electrodes are usually highly doped p-type materials. The gaps in between these single units have to be electrically controlled to maintain isolation between individual pixels, which can be achieved in a variety of ways and is dependent on the type of detector. More information about possible geometries of such setups and how they are realized, will be given in Sections 2.2 and 2.4.

2.2 The CCD

Ever since the invention of the CCD⁴ by S. Boyle⁵ and George E. Smith⁶ in 1969 at Bell Laboratories, NJ, USA, semiconductor image sensors have become the working horses of modern day astronomy. In Section 2.1.3 it was mentioned how charges are stored beneath the readout p-type layer of a photo diode, which was sideways depleted. In order to find out about the energy of the incident photon, a photon detector must transfer the information stored in each pixel to the readout electronics. In case of the CCD, Boyle and Smith found a way to move charges to one side of the detector - pixel by pixel - until they reach the readout electronics and can be manipulated. The basic structure of a CCD is equal to the pixelated structure described in Section 2.1.4. In case of the CCD, the separation of single pixels is achieved by introducing highly doped n-type injections in the p-type material (so-called *channelstops*), causing the initially homogeneous material to be divided into multiple stripes (see Figure 2.4). Attached to these stripes are multiple electrodes, which are divided into groups of three, with two outer and one inner electrode. By applying a negative potential ϕ_{low} to the two outer electrodes and a positive potential ϕ_{high} to the inner electrode, electrons will be held in a potential well underneath the inner electrode of each pixel and will therefore

⁴Charge-Coupled Device.

⁵Willard Sterling Boyle (*1924) is a Canadian physicist and recipient of the Nobel Prize in physics in 2009.

⁶George Elwood Smith (*1930) is a US applied physicist and recipient of the Nobel Prize in physics in 2009.

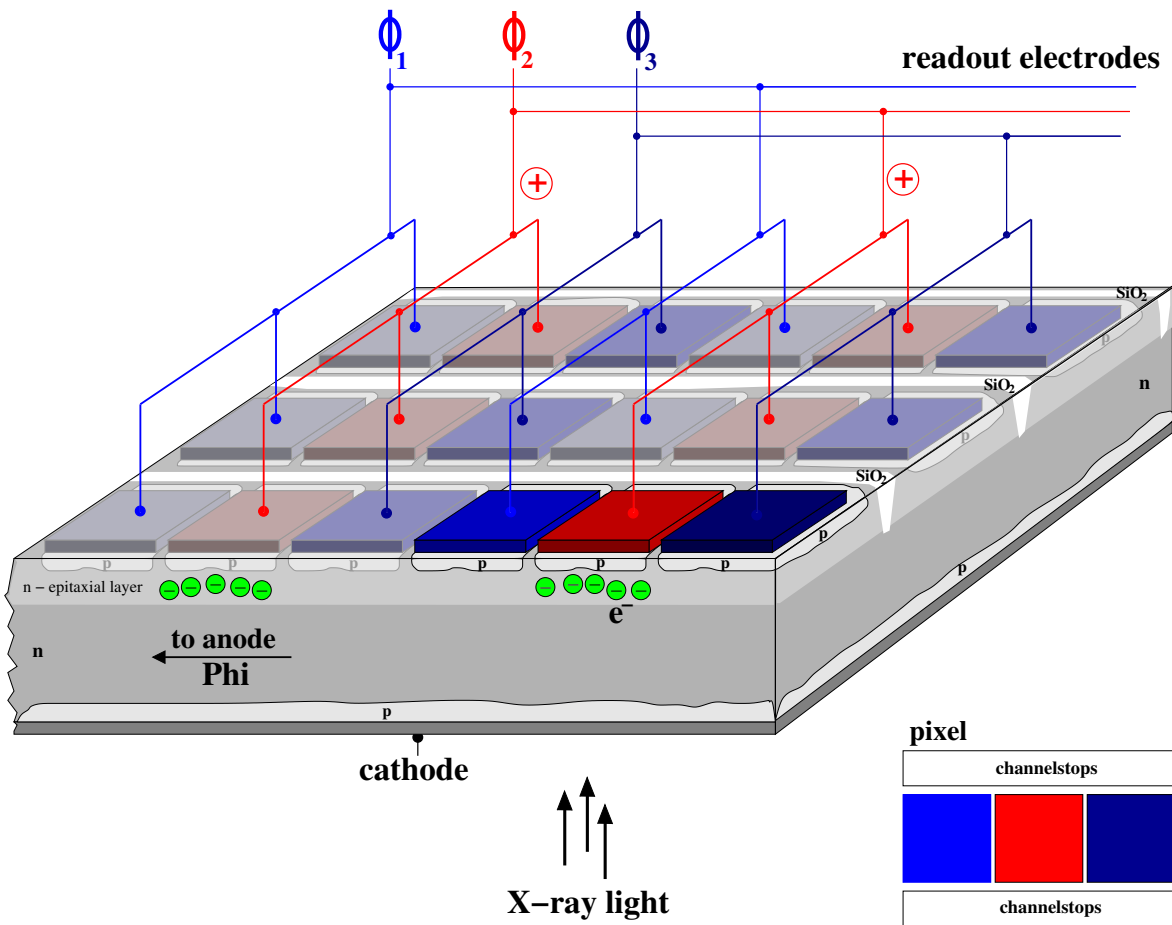


Figure 2.4: Schematic representation of a CCD. Each pixel is covered by three readout electrodes (bright blue, red and dark blue), which are connected to their corresponding ϕ -pulses. The homogeneous p-type layer is divided into stripes by channelstops, which are caused by SiO₂ into the material. The transfer direction of charges is to the left in this example, while the irradiation with X-rays happens from the bottom (backside illumination). Image courtesy of Thomas Schanz, IAAT

be separated from electrons, which were created underneath neighboring pixels. Changing these potentials, which are called ϕ -pulses, in a certain way (see Figure 2.5) can move the *charge clouds*, which have gathered underneath each pixel, towards the readout electronics of the CCD, one row of pixels at a time. The effectiveness of this movement is called *Charge Transfer Efficiency* (CTE) and measures the loss of signal charge per pixel transfer. Various types of CCD-based semiconductor detectors are currently operated by successful missions like Chandra and XMM-Newton (NASA, 2011a) or will be used in future missions like *eRosita*⁷, which is scheduled to be launched in 2012 (Cappelluti et al., 2010).

⁷extended ROentgen Survey with an Imaging Telescope Array. eROSITA is an X-ray telescope developed by the Max Planck Institute for Extraterrestrial Physics in Garching, Germany. At the heart of the mission a photon imager called the Framstore pn-CCD will detect photons up to 10 keV energy. (Cappelluti et al., 2010)

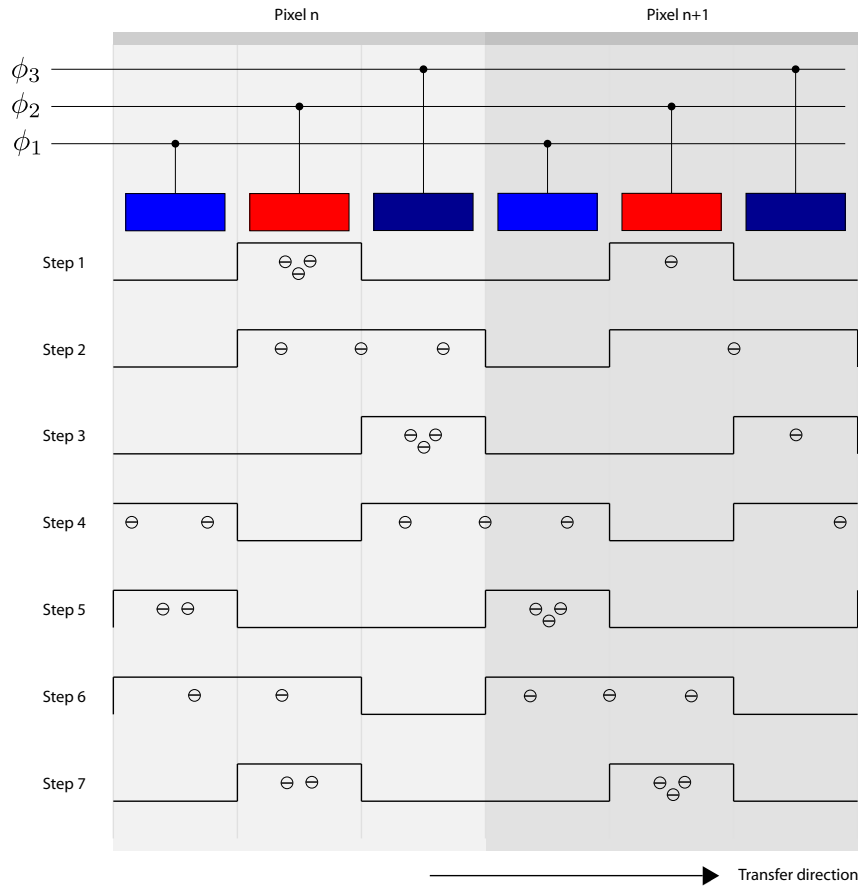


Figure 2.5: An example of the sequence of ϕ -pulses needed to transfer three electrons from pixel n into pixel $n+1$, two electrons from $n-1$ to n and one electron from $n+1$ to $n+2$, which takes a total of seven steps. For the integration period (step 1), the outer electrodes of each pixel are set to a negative potential (ϕ_{low}) with respect to the center electrode (ϕ_{high}). When the integration is over (step 2), the positive potential of ϕ_2 is extended to ϕ_3 (the right electrode of each pixel), so that electrons can move further to the right. In step 3, ϕ_2 is turned to ϕ_{low} , so that remaining charges underneath that electrode will be repelled and move further underneath the right electrode, which is still set at ϕ_{high} . Now a configuration is reached, which is the same as during integration, with the difference, that electrons are now gathered one electrode further to the right. In step 4, ϕ_{high} is applied to both, the right electrode of pixel n and the left electrode of pixel $n+1$, so that electrons can drift further, now crossing pixels for the first time. ϕ_3 is then set to low (step 5), so that remaining electrons are completely pushed underneath the left electrode of pixel $n+1$. This pattern is now repeated once more, so that the electrons will gather underneath the center electrode of pixel $n+1$ (steps 6 and 7). Using this principle, charges can be moved throughout the whole CCD line by line (pixels in one line can all be transported in parallel).

2.3 The Field-Effect Transistor

The *Field-Effect Transistor* (FET) is based on the functionality of a pn-junction and consists of three distinct regions with alternate doping, which are called *source*, *gate* and *drain*. The most common type of FET is the *Metal-Oxide-Semiconductor Field-Effect Transistor* (MOSFET), where the metal contact above the gate region of the transistor is separated from the semiconductor substrate by a thin oxide layer, which acts as an electrical insulator between the two areas (refer to Figure 2.6). For a p-type MOSFET, the gate material is an n-type material while source and drain are p-type semiconductors. If a positive voltage (which exceeds a certain threshold) is applied to the gate contact, mobile electrons from the n-type substrate are repelled from the surface. At the same time, the majority carriers of the two p-type regions are attracted to the surface, thus creating an area beneath the gate that behaves as if it was p-doped due to the majority of positive charges. This area is also called a *p-channel* or *inversion layer*. If a voltage is applied between the source and drain contacts, while the p-channel exists due to a sufficient gate voltage, a current can travel from one contact to the other through the channel. A field-effect effector can therefore act as a simple switch and has manifold areas of application.

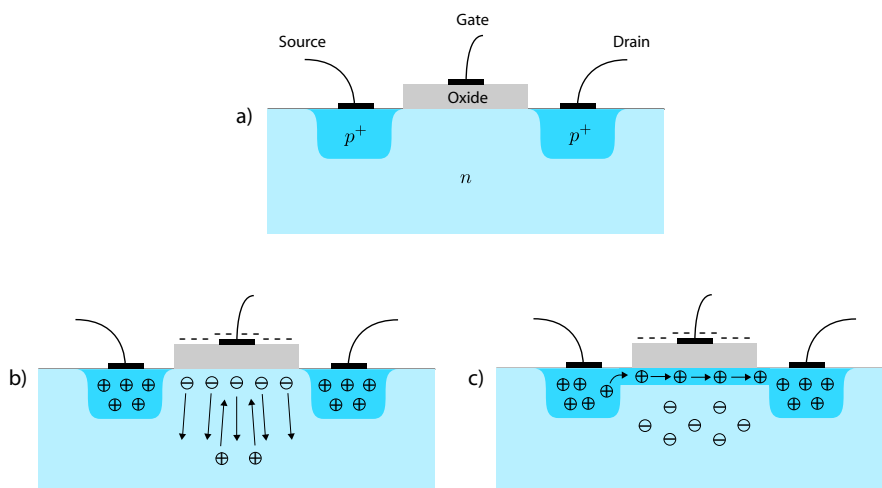


Figure 2.6: (a) Schematic representation of a p-channel MOSFET. The n-doped bulk material contains to areas of p-doped semiconductor material, which are contacted to two electrodes, the source and drain contacts. In between these areas, the gate contact is placed on top of the bulk material, but is isolated with an oxide layer. (b) If a negative voltage is applied to the gate contact, electrons will be repelled from the surface, while holes will be attracted. (c) Shortly after a negative voltage was applied to the gate contact of the MOSFET, a conducting p-channel will have formed, allowing charges to flow from the source to the drain contacts, thus connecting them like a switch. (Turton, 2000)

2.4 The DEPFET

Based on the field-effect transistor, the semiconductor labs (HLL) at the *Max Planck Institute for Extraterrestrial Physics* (MPE) have developed a new type of photon detector, the so-called *Depleted P-channel Field Effect Transistor* (DEPFET), whose concept was first introduced in 1987 by Kemmer and Lutz (1987) and combines a variety of unique characteristics. Since it is the fundamental building block of the WFI onboard of IXO, its geometry and operational principles will be introduced in detail in the following sections.

2.4.1 Geometry and Operation Principle

The *Depleted P-channel Field Effect Transistor* (refer to Figure 2.7) is in principle an implementation of an *Active Pixel Sensor* (APS), which means, that it has its own amplification circuit built in. The p-channel readout FET (with a circular gate structure) is integrated on the surface of a highly n-doped silicon substrate, which is sideways depleted as described in Section 2.1.3. Similar to a CCD, the two corresponding external biasing voltages are chosen in a way, that creates a potential minimum for electrons near the surface of the pixel and close to the FET structures, which are integrated on top (also called the front-side). Electron-hole pairs created in the bulk material are separated by the electrical field, which is due to the backside voltage between both p-doped sides of the DEPFET. In order to confine generated electrons in the direction parallel to the interface of bulk material and FET structures, a small n-doped region, called the *Internal Gate* (IG), is introduced underneath the gate electrode. A charge cloud will therefore be confined to an area underneath the channel of the FET and cannot leak into other pixels. The presence of charges in the proximity of the p-channel is the key-element for read-out of the DEPFET. At a certain gate voltage V_g a p-channel will form and a constant current I_{ch} will flow from source to drain of each pixel. If electrons are located in the internal gate, they will induce positive mirror charges in the channel, thus altering its conductivity and also the current I_{ch} . The transconductance g_q relates the presence of the electron charges in the internal gate δq_{IG} to the resulting change of I_{ch} .

$$g_q = \frac{\delta I_{ch}}{\delta q_{IG}} \quad (2.3)$$

Consequently, the change of I_{ch} is a measure for the number of mirror charges in the channel and therefore a measure of the number of electrons stored in the internal gate. Furthermore, the number of electrons is a measure of the photon energy incident in the pixel, allowing an indirect measurement of the photon energy via the channel current I_{ch} . The biggest advantage of the DEPFET is, that electrons, created by radiation, do not have to be moved around within the detector, thus causing no charge transfer inefficiency as in the case of the CCD. Moreover, the readout can be executed multiple times (called *sampling*) without altering the electrons in the internal gate, which according to Treis et al. (2008) can store up to 10^5 electrons. Due to the FET structure and the measurement of I_{ch} as a measure of the created electrons, the first amplification of the signal is already conducted on site. Since the DEPFET is backside illuminated, the damageable frontside is screened from incoming radiation, thus making the device radiation hard and interesting for space-related application.

Since electrons in the internal gate are not transported, they will stay there indefinitely. For clearing purposes of a DEPFET pixel, a highly n-doped clear contact is implemented into the

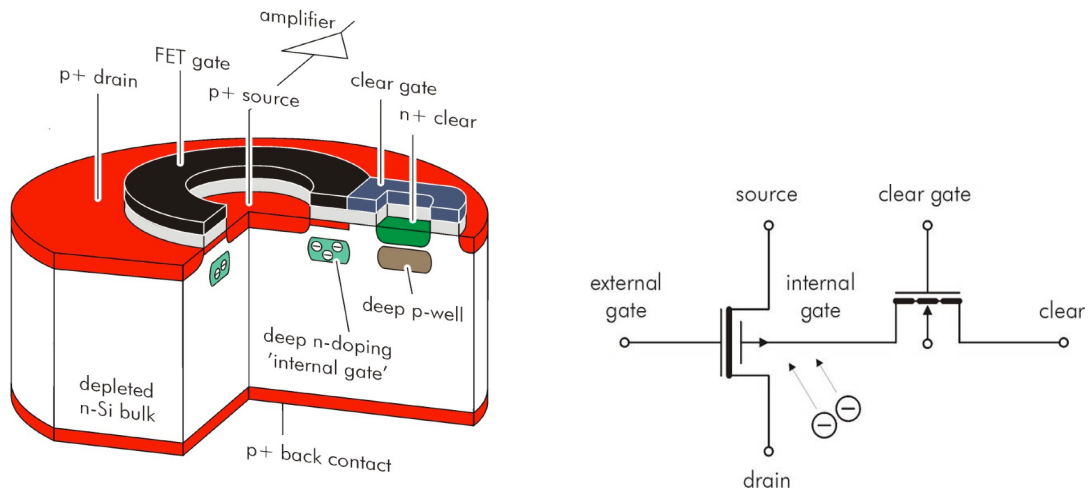


Figure 2.7: Layout of a DEPFET pixel. A fully depleted n-doped Si bulk (white) is sandwiched between two strongly p-doped layers, one that serves as the drain contact for the readout FET and one back contact. The circular FET structure (black) is isolated from the top p-layer by an isolating oxide layer (grey). Underneath the FET gate ring structure, the internal gate (turquoise) is located. On the right hand side on the top, the rectangularly clear gate structure (blue) is located, also isolated by an oxide layer. Inside of this structure, the clear contact can be seen, together with the deep p-well (green) situated underneath. On the right hand side, next to the DEPFET layout, a schematic representation of the two combined FETs in a DEPFET can be seen. (Lechner, 2006)

bulk material, where a positive clear voltage V_C can be applied, in order to remove electrons from the internal gate. To prevent electrons from leaking from the internal gate into the clear contact during integration, the clear contact itself is surrounded by a rectangularly shaped clear gate FET structure, sharing the source contact with the readout FET (also called a parasitic FET). In principle, it can be described as a n-channel MOSFET which creates a conducting n-channel from the internal gate to the clear contact if an appropriate *clear gate voltage* V_{CG} is applied. During integration intervals, the clear gate is kept at a negative voltage, creating a potential barrier between the clear contact and the internal gate, in order to prevent charge injection from the highly n-doped clear contact. On the other hand, during integration, charges could flow directly to the clear contact instead of the internal gate. In order to prevent such movements, the clear contact is screened from the bulk material by an additional p-doped area, called a *p-well*. It has to be noted, that the DEPFET cannot detect radiation during the clearing process, since generated electrons would directly move from the internal gate into the clear contact. Consequently, the detector has a *dead-time* for the clearing period, thus making it necessary to minimize the time, which is needed for this operation.

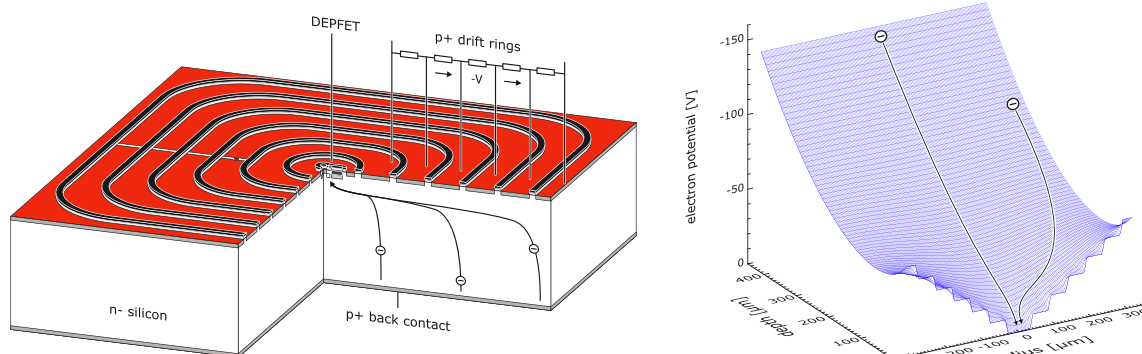


Figure 2.8: Macropixel design of a DEPFET pixel. By introducing drift rings (black) into the p-layer on top of the Si-bulk and applying increasing negative voltages from the outside to the center, a field configuration (right hand illustration) can be achieved, that will "push" electrons generated anywhere within the pixel towards the readout FET. (Lechner et al., 2008)

2.4.2 Macropixel

One goal of designing a photon detector for a satellite mission, is to have pixel sizes on the order of the *Point Spread Function* (PSF) and angular resolution of the focussing optics. The most important reason for this is, that an oversampling of the PSF with many pixels will generate high data loads and unwanted aliasing effects. For point sources, it is much more useful to detect all incoming photons in one single pixel, which will simultaneously reduce the readout time of the localized information. In order to achieve such configurations, the actual pixel size of a DEPFET detector can be increased by using of so-called *drift rings*, which will extend the photon collection area of a pixel and convert it to a so-called *macropixel* (see Figure 2.8) structure. Lechner (2006) show, that pixel sizes with an edge length of up to 1 cm are possible. Drift rings introduce a radial field component within the bulk material of the DEPFET and are biased with an increasing negative voltage from the center to the outside. Electrons which are generated somewhere in the bulk material will drift towards the minimum potential, thus traveling from the outside to the center of the pixel, where the DEPFET gate and clear gate structures are located. The utilization of macropixels is also foreseen for the WFI onboard of IXO and more information about their size will be given in Section 3.2.3.

2.4.3 Read-Out Electronics for DEPFET Matrices

Since DEPFETs are used in pixelated photon detectors, they are usually combined into large monolithic arrays. The readout of these arrays, which will have 1024 by 1024 DEPFETs in case of the WFI, can be achieved by using effective connection schemes. For the WFI, all pixels of the detector are located on top of a common Si bulk, which will be irradiated from the homogeneous back side, thus having a *fill-factor* of 100%. For the simultaneous operation of whole lines of the detector, the *gate* and *clear gate contacts* of each single DEPFET pixel are interconnected and controlled by a common voltage (Figure 2.9 shows an example of a 4x4

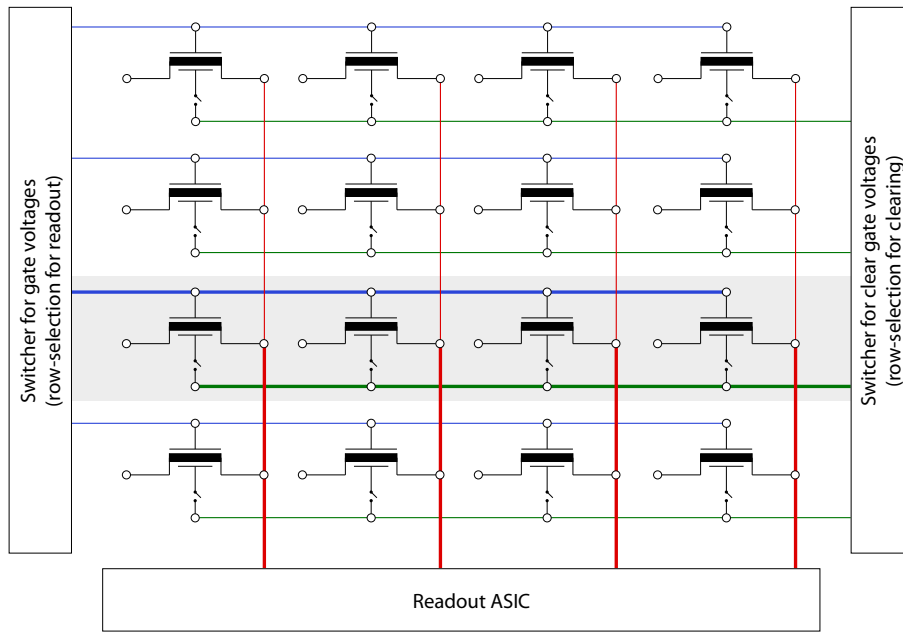


Figure 2.9: An array of 4 x 4 DEPFET structures, which are interconnected row-wise. On the left and right-hand side are the switcher electronics for readout and clearing operations respectively. The broad lines indicate connections which are active for the grey-shaded row (3rd from the top). At the bottom, the readout ASIC is located, which processes all pixel information of one row in parallel. (Lutz, 2005)

DEPFET pixel array). On the left and right hand sides of the array, the so-called *switcher ICs* are located, one for the control of the readout and one for the control of the clear process. On the bottom of the array, the read-out ASIC⁸ is located, which will amplify the signal of all pixels of one line in parallel. The readout of each line is conducted by biasing the gates of one row with a voltage $V_{G_{on}}$, while the gates of all others rows are biased with the voltage $V_{G_{off}}$, thus having no conductive p-channel. After the p-channels of the selected row have been created by the corresponding gate voltage $V_{G_{on}}$, the channel current I_{ch} of the DEPFETs is measured. After this information has been stored, the same line is cleared by applying the clear gate voltages V_{CG} to all pixels. Afterwards, $V_{G_{on}}$ is again applied to the selected row in order to measure I_{ch} of each pixel without any electrons present in their internal gate. This *baseline level* is subtracted from the first measurement, thus revealing information of the number of generated electrons in each pixel. After the readout is finished, the gates of the current row are turned off, and the next row will be selected. All parallel processed signals of one row are serialized in a multiplexer stage within the readout ASIC, before they are passed on to an *Analog Digital Converter* (ADC) and furthermore processed by digital electronics, like the EPP.

⁸*Application Specific Integrated Circuit*. ASICs are integrated circuits, which are designed for one specific operation.

3 The International X-ray Observatory

The very successful Chandra and XMM-Newton X-ray missions were both launched in 1999 and have delivered terabytes of valuable information in an energy band of approximately 0.1 - 15 keV. Considering the development time-spans of modern detector systems and the fact, that these two missions have been in operation for more than 10 years, new X-ray missions with improved characteristics are being developed, in order to push the limits of measurable energies and flux rates even further. One of these missions is the International X-ray Observatory, which is a joint-effort of NASA, ESA and JAXA to create the next-generation X-ray space telescope. Currently, IXO is proposed as an *L-class mission* candidate for ESA's *Cosmic Vision Programme* (CVP), which will be introduced in Section 3.1.1. Historically, IXO's origins can be traced back to two separate X-ray missions - the *X-ray Evolving Universe Spectrometer* (XEUS) and *Constellation-X* (Con-X) - designed by ESA and NASA respectively. Due to budgetary reasons, these two missions were merged in summer 2008, when first IXO studies commenced. (Nousek et al., 2009)

In Section 3.1 the historical developments leading to the proposal of IXO are revisited, while Section 3.2 will focus on the initial requirements of the mission and its technical implementation. Since IXO is currently in *phase A* of its studies, many of these aspects are **subject to change** as the study progresses. A short overview of the current status of the mission will therefore be given in Section 7.4. Summing up the chapter, the last section will motivate the usage of an EPP and present calculations concerning the expected data rates for the WFI.

3.1 Historic Origins of IXO

3.1.1 The Cosmic Vision Programme

Science has reached a state in which still open questions are mostly very complex and in which theories cannot be probed with simple, small-scale experiments anymore. The *Large Hadron Collider* at CERN¹ is one prime-example of how the search for the origin of our existence has led to the conduction of experiments and missions, that will occupy hundreds or even thousands of scientists for many years to come. Astronomy makes no exception in this development, but marks the forefront of ever increasing mission sizes and expenses. In order to cope with these issues, space agencies have realized, that long-term planning is fundamental and have shifted their studies to so-called *agendas*. Such planning has already been conducted by ESA for example, with the *Horizon 2000* and *Horizon 2000 Plus* studies from 1984 and 1994 respectively. Currently, the CVP represents ESA's agenda for the years of 2015 - 2025. At its core, the CVP formulates four key questions, which cover a wide-range of astrophysical topics. Encouraging interdisciplinary exchange between scientific fields, these

¹Conseil Européen pour la Recherche Nucléaire. Represents an international organization, whose purpose is to operate the world's largest particle physics laboratory in Geneva, Switzerland.

questions equally appeal to astrophysicists as well and astrobiologists, astrochemists, etc. In order to investigate possible answers, ESA also proposed which scientific observations could be useful.

What are the conditions for planet formation and the emergence of life? For question number one, ESA proposed the mapping of stars and planets by peering into the highly obscured gas-clouds in which they form. The search for *exo-planets* and other stellar systems, as well as measuring possible *bio-markers* in their respective atmospheres, was suggested as one crucial aspect of research. Furthermore, the *in-situ* exploration of terrestrial planets² our Solar System and the investigation of their solid surfaces, in order to find environmental conditions, that could support life, was proposed as a possible research scenario.

How does the Solar System work? Question number two focusses on our Sun and the *jovian planets*³. ESA suggests to study the plasma and magnetic field environments around Earth and Jupiter, as well as the Sun's poles, reaching as far as the *heliopause*⁴. Lastly, *Near-Earth Objects* (NEOs) like *asteroids* and other small bodies should be directly sampled in order to shed light on the fundamental physical processes in our Solar System.

What are the fundamental physical laws of the Universe? For question number three, ESA suggested to use the stable and weightless environment of space to conduct experiments, which could reveal tiny deviations from the current *standard model of fundamental interaction*. Additionally, they push the idea of gravitational wave astronomy, in order to detect the gravitational radiation background of the *Big Bang*. In their opinion, the investigation of matter under extreme conditions, such as black holes and other compact objects, could be one way of research to probe gravitational theory in very strong field environments and reveal the equation of state of matter at *supra-nuclear energies* in neutron stars.

How did the Universe originate and what is it made off? Question four finally addresses the past and future of the Universe. Scientists are asked to define the physical processes, that led to the *inflationary phase* of the early Universe and to investigate the nature and origin of *dark energy*, which is supposed to be the reason for its accelerated expansion. Furthermore, ESA stresses research, that might shed light on the first gravitationally bound objects and their evolutionary tracks until today. Finally, they want to trace the formation and evolution of SMBHs in relation to their host galaxies and *star formation* and also investigate the life cycles of matter in the Universe.

The following sections will focus on the XEUS and Constellation-X missions, which were originally proposed to operate within the framework of one or more of these questions.

²The term terrestrial planets refers to all planets with a solid surface, which are the four innermost planets, Mercury, Venus, Earth and Mars.

³The term jovian planets refers to all gas planets in the Solar System, which are the four outer planets Jupiter, Saturn, Uranus and Neptune.

⁴The term heliopause describes the area in our Solar System, where the pressure due to the Solar wind and the interstellar medium compensate each other.

3.1.2 X-ray Evolving Universe Spectrometer

As a potential follow-up to XMM, the X-ray Evolving Universe Spectrometer mission was originally proposed by ESA in 1999. In the context of ESA's CVP, it focussed on two of the four fundamental questions, namely "What are the fundamental physical laws of the Universe?" and "How did the Universe originate and what is it made of?". The original plan was, to place XEUS into an L2-orbit, since it provided a stable thermal environment for temperature control of the optics and the instruments, as well as an *eclipse free view* of the Universe. Furthermore, the *benign gravity gradient* was a key aspect, since XEUS wanted to reach a long focal length of around 35 m by *formation flight* principle (see Figure 3.1). For this purpose, a designated *Mirror Spacecraft* (MSC) and a *Detector Spacecraft* (DSC) had to fly in a stable formation within an accuracy of 2.5 mm along the optical axis and 0.5 arcsec absolute attitude measurement. Weak gravitational fields were needed in order to economically sustain this formation without using too much fuel for realignment maneuvers.

The DSC of XEUS was supposed to be equipped with a total of five focal plane instruments, one of which was a *Narrow Field Imager* (NFI) based on superconducting *transition edge detectors* in an energy range of 0.1 - 20 keV and a 2 - 6 eV energy resolution at 0.1 - 8 keV respectively. The field of view (FOV) was designed to be approximately 1.6 arcmin square. Complementary to this instrument, a *Wide-Field Imager* (WFI) was planned, which should have been realized as a *silicon pixel array*, sensitive in an energy range of 0.05 - 20 keV, with an energy resolution of 30 - 150 eV and a FOV of 7 arcmin. The WFI would have been supplemented with an additional *Hard X-ray Imager* (HXI), extending the energy range of the WFI up to 40 keV.

The three remaining supplement instruments were the *High Timing Resolution Spectrometer* (HTRS), which was supposed to measure sub-millisecond variations in the emissions of Black Holes and Neutron Stars, as well as the *X-ray Polarimeter* (XPOL), which should have been the first instrument to measure the *polarization* angles of X-rays.

Concerning the optics, the original plan was to utilize *silicon micro-pore optics*, in order to build light-weight mirrors, which could supply an effective aperture of 5 m² at 1 keV and a spatial resolution of 5 arcsec *Half-Power Diameter* (HPD).

However, with all these ambitious goals and state-of-the-art instrumentation, XEUS fell outside of the cost-envelope for even L-class missions. As a result, international participation was required for the realization of the mission, which was one the reasons why the original proposal XEUS was eventually discarded.

3.1.3 Constellation-X

Similar to ESA, also NASA has an agenda planning the scientific development of the agency in a timeframe of 2003 until 2028. It is called *Beyond Einstein* and identifies three science objectives for the topic of "Structure and Evolution of the Universe" (Hertz, 2003), which are "Find out what powered the Big Bang", "Observe how black holes manipulate space, time, and matter" and "Identify the mysterious dark energy pulling the Universe apart". A proposed mission to realize these objectives was Constellation-X, which was originally planned as a *multi-satellite mission* (refer to Figure 3.2), but was re-examined due to increasing launch-vehicle cost and changed to be comprised of one single spacecraft. Con-X had two distinct telescope systems operating in slightly overlapping energy ranges. The *Spectroscopic X-ray*

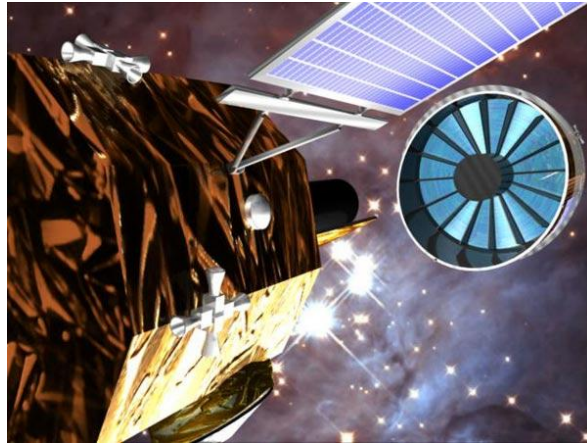


Figure 3.1: An artist's impression of the XEUS mission in flight. In the foreground the DSC can be seen, being in formation flight with the MSC. The mirrors of the MSC are shielded by a baffle against stray light. (Arnaud et al., 2009)

Telescope (SXT) was supposed to operate in the range of 0.3 - 10 keV, while the *Hard X-ray Telescope* (HXT) would have operated within 6 - 40 keV. Four SXT units were planned to be carried by Con-X, each of which consisted of a *Flight Mirror Assembly* (FMA) with 10 m focal length (made of 168 tightly nested Wolter-I mirror shells) and an *X-ray Microcalorimeter Spectrometer* (XMS). Furthermore, two of the SXTs would have utilized *X-ray Grating Spectrometers* (XGS), feeding a CCD array for lower energies. By distributing the whole effective area of the telescope onto four smaller telescopes, weight and dimensions were considerably reduced and the assembly of the mirror module was simplified.

The HXT was planned to be comprised of one or two *grazing incidence* nested mirrors, feeding a CdZnTe detector for the higher energies of the observatory's bandpass.

The main differences between the SXT and the HXT mirrors were, that the radial dimensions of the HXT mirrors were significantly smaller than for the SXT mirrors, since highly energetic photons require smaller grazing angles for effective reflection. Also, in contrast to the SXT mirrors, they needed to be specifically coated (in order to allow the reflection of high energy photons up to 40 keV) and their angular resolution requirements were less stringent.

One crucial aspect of Con-X was the redundancy of most systems, since it retained the mission's robustness against failure of single components. Also, many instruments could have worked simultaneously, which is a key aspect when studying high energy processes, since they can be variable on very short time-scales.

Equal to XEUS, Con-X would have been launched into an L2-orbit, in order to provide a thermally stable environment as well as a low particle background and an eclipse-free FOV. The mission lifetime was planned to be 5 years, with sufficient consumables for a 10-year lifetime. (Bookbinder et al., 2008)

3.2 The IXO Mission

As already mentioned, neither XEUS nor Con-X were realized as separate missions, but were merged due to their large technical overlap and their individual high costs. In 2008, IXO was



Figure 3.2: An artist's impression of original Con-X mission, which was planned to be a multi-satellite mission at first, but was redesigned into a single satellite mission. Here, four Con-X satellites are shown in formation flight, aiming at the same source to make use of their combined larger effective area. GSFC/NASA

proposed as the next large-scale X-ray observatory and therefore as a successor to Chandra and XMM. It has adapted several aspects of both XEUS and Con-X and directly profited from the work, that had already been done for these two missions. Also, with the *Japanese Aerospace Exploration Agency* (JAXA) another international member joined the collaboration and will support the mission with its know-how and technical expertise.

The following sections will focus on the scientific goals of IXO, the mission design and parameters, as well as technical aspects of each individual instrument onboard. Most of the information presented is taken from Bookbinder (2010).

3.2.1 General Parameters

Since IXO is proposed as a successor of Chandra and XMM, it will have considerably improved characteristics and technological improvements will push the limits for detecting even fainter sources at even higher energies. As the first satellite of its class, IXO will be able to focus X-ray photons up to 40 keV and conduct imaging studies in this energy band. In order to achieve the needed focussing power with a large diameter grazing incidence Wolter-I type telescope, IXO will have a focal length of 20 m. Unfortunately, such values cannot be achieved easily due to issues of size and weight. A first solution to this problem was investigated with a mission proposal of XEUS, which suggested to divide the mission into two spacecrafts, one carrying the FMA and one carrying the instruments and align them via formation flight. This idea however has been discarded for IXO, since its *Technological Readiness Level* (TRL) was too low and the connected risks too high. Instead, the Japanese space agency JAXA will support the project with an *Extendable Optical Bench* (EOB), which was inherited from past missions of the agency. In principle, the EOB is a foldable connection between the *Instrument Module* (IM) and the FMA, thus connecting them into one single spacecraft, while at the same time shielding the detector focal plane from stray light. The necessity for such a construction arises from the fact, that modern day *carrier rockets* like an *Ariane V* cannot accommodate structures as large as IXO, when it is fully deployed (see Figure 3.3). The FMA will provide an

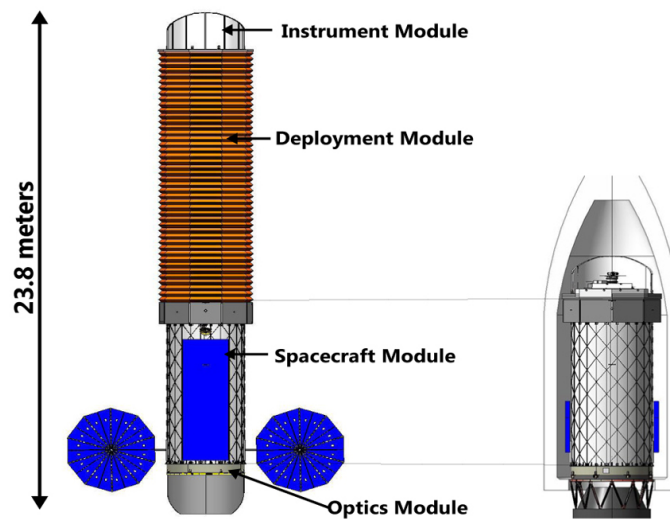


Figure 3.3: Image of IXO and Ariane rocket. The left images shows IXO fully extended to its length of over 23 m. The image on the right shows IXO with folded EOB, which enables the fitting of the satellite into the Ariane carrier rocket. (Bookbinder, 2010)

effective area of 30000 cm^2 at 1.25 keV, 6500 cm^2 at 6 keV and still 150 cm^2 at 30 keV. IXO will aim for an angular resolution of 5 arcsec HPD, which is three times better than the angular resolution of XMM, but also about 10 times worse than Chandra. With its enormous effective area however, IXO will surpass both, XMM and Chandra, by orders of magnitude throughout the whole detectable energetic range and even extend this range into the high energy band of 20 - 40 keV (compare Figure 3.4). IXO will be launched into an L2-orbit, for the same reasons that were foreseen for XEUS and Con-X. It is designed for a mission lifetime of 5 years, but will carry consumables for at least 10 years.

3.2.2 The Optics of IXO

As already mentioned, IXO will have an angular resolution of 5 arcsec. In order to meet these requirements, the PSF of the FMA needs to be at 4 arcsec or better, a criteria which is currently missed by a factor of 3, rendering the mirror development as the current bottleneck of the mission. In order to reduce the risk of not meeting these requirements in time, IXO is currently pursuing two different technologies simultaneously, to produce light-weight, yet high-performance mirrors, which will lead to a highly modular mirror design. With this modular approach, a common interface between the FMA and the EOB can be used, thus making it possible to utilize either one of the different technologies onboard of IXO.

Thermally Formed Segmented Glass Mirrors

Thermally formed segmented or "slumped" glass mirrors, are fabricated by thermally deforming commercially available, 0.4 mm thick sheets of glass. For this purpose, they are placed on a *precision-figured forming mandrel* and then heated up to 600°C . As a result, the glass will become soft and wrap around the mandrel under its own weight (see Figure 3.5 for illustra-

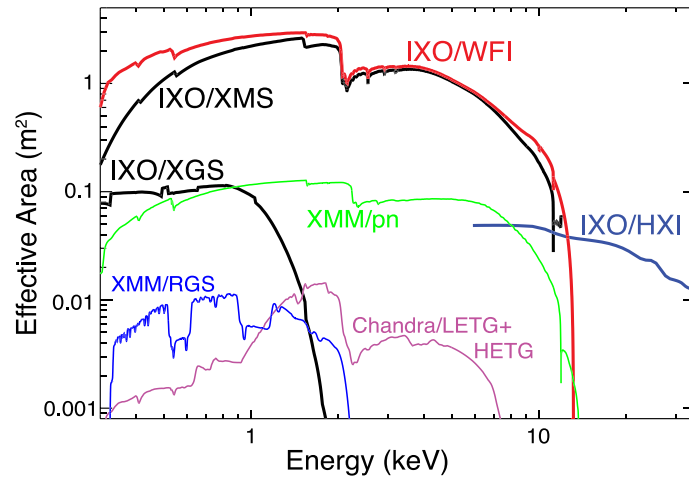


Figure 3.4: IXO effective area of instruments vs. other important X-ray missions. (Bookbinder, 2010)

tion). Afterwards the glass sheet is annealed and cooled down to room temperature. Once the glass has cooled down, it is cut to a prescribed size to meet requirements for its integration into a precision housing. Finally, its reflecting surface is coated with iridium to enhance its reflectivity for X-rays .

Aligning individual mirror segments is the biggest problem after they have been manufactured, since they are not completely stiff and can deform under their own weight. Consequently, they are put into a temporary housing, where segments are bonded at a number of points along their edges to a rigid structure and can be used for full-illumination tests. Once the correct alignment is found and tests show results within the specifications, the segments are finally bonded to a permanent mount.

So far, optical performances of 15 arcsec HPD have been achieved, but further improvements in the quality of the mandrels, alignment and coating have to be made in order to reach the requirements for IXO. (Zhang et al., 2008)

Silicon Pore Optics

Silicon Pore Optics use commercially available double-sided high grade 12" Si-wafers, which are manufactured by the semiconductor industry and diced into individual plates, which will later on form the mirrors when stacked together (see Figure 3.6). Afterwards, their backside is grooved and will have 0.17 mm ribs with a pitch of 1 mm. These numbers however are subject to change, since they can be adjusted to optimize the optical performance and the mechanical behavior of a stack. During all operations on the wafers, the initial surface roughness has to be preserved, which is achieved by using protective layers on untouched areas. The sidewalls, which arise from the grooving of the backside are covered with a non-reflective material, to reduce influences from stray-light. The reflective and ungrooved other side of the mirror is coated with a patterned iridium coating, keeping areas, where additional mirror structures will be mounted on, free of the coating. Single mirror plates are furthermore cleaned and elastically bent into a conical shape by a fully automated stacking robot in a very clean environment. The achievable angular resolution is limited by the height of a single pore and

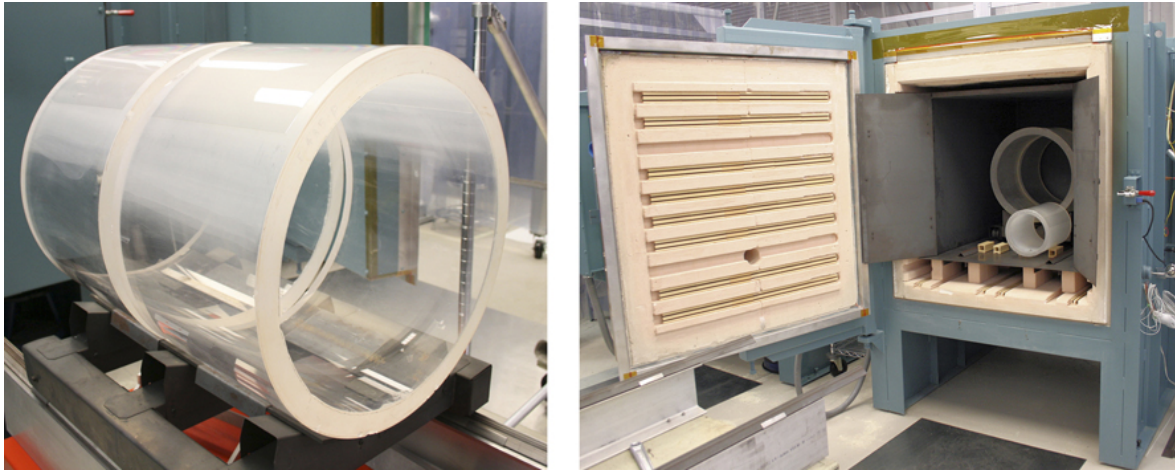


Figure 3.5: Left image shows a slumped glass sheet on a mandrel after it has been thermally fit to the surface. Right image shows the heating ovens in which the initially straight sheets of glass are heated to wrap around the mandrels. (NASA, 2011b)

reaches a minimum value of 3 arcsec HPD for pore-heights of 0.6 mm and IXO's 20 m focal length. Due to the inherent stiffness of the mirror stacks, their geometry is preserved during further mounting and stacking processes. Two stacks of mirrors are co-aligned and integrated into so-called *mirror-modules*. Since the first fully demonstrated production chain, further improvements in the stacking techniques have led to a current performance of 10 arcsec HPD for SPOs. (Collon et al., 2010)

3.2.3 Instruments Onboard IXO

IXO will host a total of five instruments on its *Fixed Instrument Platform* (FIP), which is part of the IM. Furthermore, it will have a *Moveable Instrument Platform* (MIP) in the focal plane, which will enable the observatory to move single instruments into the beam of focussed X-ray light, one at a time (refer to Figure 3.7). Consequently, simultaneous observation of multiple instruments is not possible for MIP instruments, but each instrument will be exposed to the whole incoming *X-ray flux*. Part of the incoming photon flux however, is distributed to the fifth instrument, the *X-ray Grating Spectrometer* (XGS), by a reflective grating. The XGS is located aside from the MIP and will be working in parallel of any observation, no matter which instrument is in use. All of the instruments planned for IXO will be presented in detail in the following sections, with a special emphasis on the WFI.

X-ray Grating Spectrometer (XGS)

As already mentioned above, the XGS (Figure 3.8) will be located aside from the MIP in order to operate with part of the incoming photon flux at all times. It will consist of newly developed, high efficiency *blazed transmission gratings*, also called *critical-angle transmission* (CAT) gratings, which combine the advantages of traditional transmission gratings and X-ray reflection gratings. They will be low mass with an extremely relaxed alignment, yet have high efficiencies due to blazing in the direction of the grazing incidence of the Wolter-I optics. The XGS will offer extraordinary energy resolution figures of $E/\Delta E > 3000$ in an energy

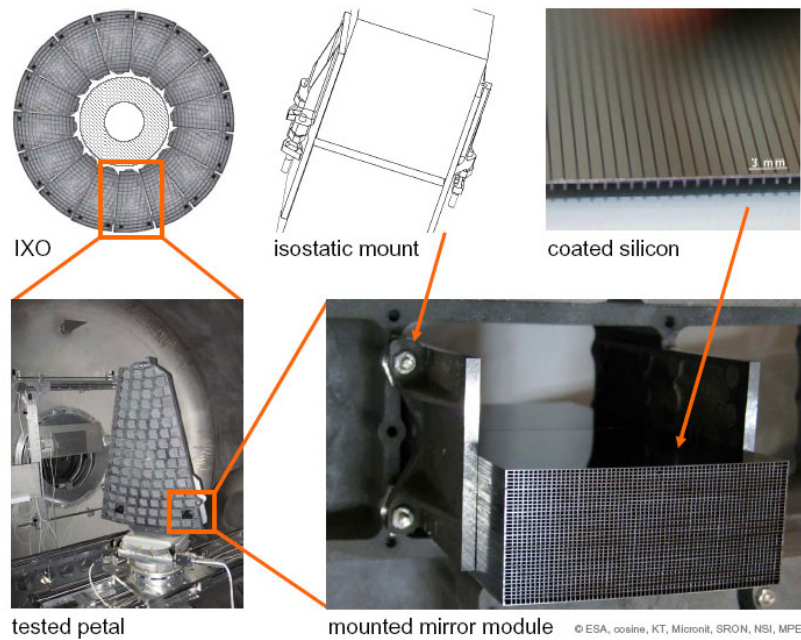


Figure 3.6: Figure shows various aspects of the production of SPO mirrors for IXO and their assembly into stacks for mirror segments. (NASA, 2010)

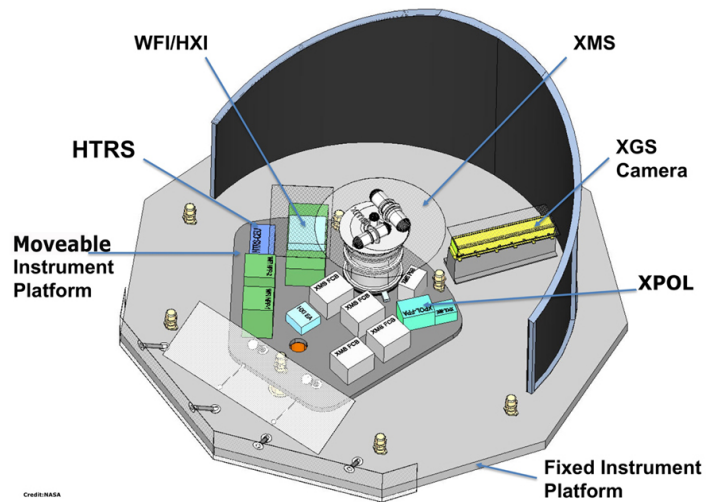


Figure 3.7: Schematic representation of the moveable instrument platform. The instruments are located on a turnable table and are shielded from stray light by a baffle. The moveable instrument platform is located on the fixed instrument platform. (NASA, 2011b)

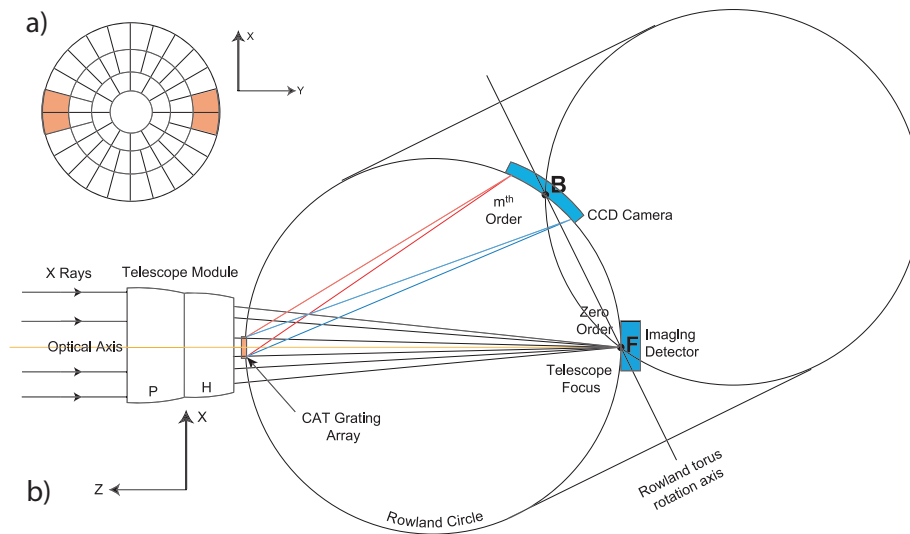


Figure 3.8: (a) Location of the CAT grating in respect to the FMA (b) Schematic representation of operational principle of the XGS. The XGS gratings will reflect part of the incoming photons onto the XGS CCD detector camera. The zero order photons will be unaffected by the grating and reach the instruments in the focal plane. (Heilmann et al., 2009)

range of 0.3 - 1 keV. Observations and spectral measurements in this soft part of the X-ray spectrum will resolve absorption and emission signatures of atomic ions and reveal valuable information about the plasmas contained in the large scale structures of the Universe or even individual stars. Diffracted light from the CAT grating is detected by a linear array of 32 backside illuminated *framestore*-style CCDs (dimensions 25 x 25 mm² at 25 μ m per pixel), which will not interfere with any other instruments onboard of IXO and can therefore operate simultaneously. A preliminary analysis of X-ray tests performed for current CAT gratings have shown blazing behavior in accordance with the prediction for photon energies up to 1.28 keV. (Heilmann et al., 2009)

X-ray Microcalorimeter Spectrometer (XMS)

The X-ray Microcalorimeter Spectrometer (Figure 3.9) was originally planned as an instrument onboard of XEUS, but was adapted by the IXO mission. It will consist of an array of X-ray micro-calorimeters with *Transition Edge Sensors* (TES). Incoming photons will heat up the superconducting material of the TES, thus triggering a sudden-rise in resistivity of the material. The resistivity change can be measured and will supply information about the incident photon. The basic geometry of the XMS consists of one outer and one inner array, which have separate requirements regarding size and resolution figures. The inner array will be a 40 x 40 pixel matrix, with a pixel size of 300 μ m square and an energy resolution < 2.5 eV. The outer array of 52 x 52 pixels of 600 μ m size, will be multiplexed to one single SQUID⁵ in groups of four, in order to keep the number of readout channels low. Major tech-

⁵Superconducting QUantum Interference Device. A SQUID is a very sensitive magnetometer used to measure very weak magnetic fields.

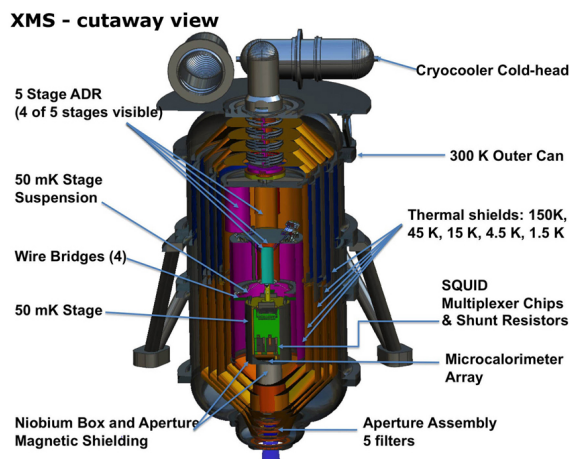


Figure 3.9: Cutaway view of the XMS: The various thermal shields can be seen with the microcalorimeter array located on the bottom behind the aperture assembly. (NASA, 2011b)

nological challenges include the reduction of cross-talk between hit pixels and a fast cool-down (therefore dead-time) if a pixel has been hit. Also, in order to reject charged particles from detection by the XMS, an *anti-coincidence detector* will be required underneath the detector. The temperature, at which the array will be operated, lies at around 50 mK and requires very low power dissipation from the surrounding electronics. (den Herder et al., 2010)

X-ray Polarimeter (XPOL)

Since the OSO-8 mission in 1975, no polarimeter has embarked on a space-based mission. Consequently, polarimetry, especially of X-ray photons, is a field still new to astrophysics and suggests to hold highly rewarding information. The XPOL instrument (Figure 3.10) will be a polarimeter based on the photoelectric-effect (refer to Section 1.4.1) and realized as a *Gas Detector* (GD) on the FIP. It will work in an energy range of 2 - 10 keV and provide polarization measurements simultaneously with angular measurements of 5 arcsec accuracy for incoming photons. Furthermore, it will conduct spectral measurements with an energy resolution of $E/\Delta E \approx 5$ at 6 keV and timing information at a few μs level. Its FOV will cover 1.5×1.5 arcmin. In principle, the GD will be a simple, $50 \mu\text{m}$ thick counter with an beryllium entrance window, filled with a mixture of low atomic number gases. A photon hitting the absorption gap, which has a size of 10 mm and is located close to the entrance window, will generate a *photo-electron* by ionizing the absorptive material and transforming the rest of its energy into the electron's kinetic energy. The interaction of the photo-electron with the gas mix inside the detector chamber will produce a track of electron-ion pairs close the impact site. Electrons from these pairs are accelerated by an electric field towards a *Gas Electron Multiplier* (GEM), which is in principle a *Micro Channel Plate* (MCP). Each hole will amplify the incoming charge, thus amplifying the track as a whole and preserving information about the shape and the charge. Further analysis of these tracks will allow the determination of the exact impact point (with an accuracy of $150 \mu\text{m}$ FWHM) and the ejection direction of the primary photo-electron. The latter carries the information about the polarization direction of the incident photon. (Costa et al., 2008)

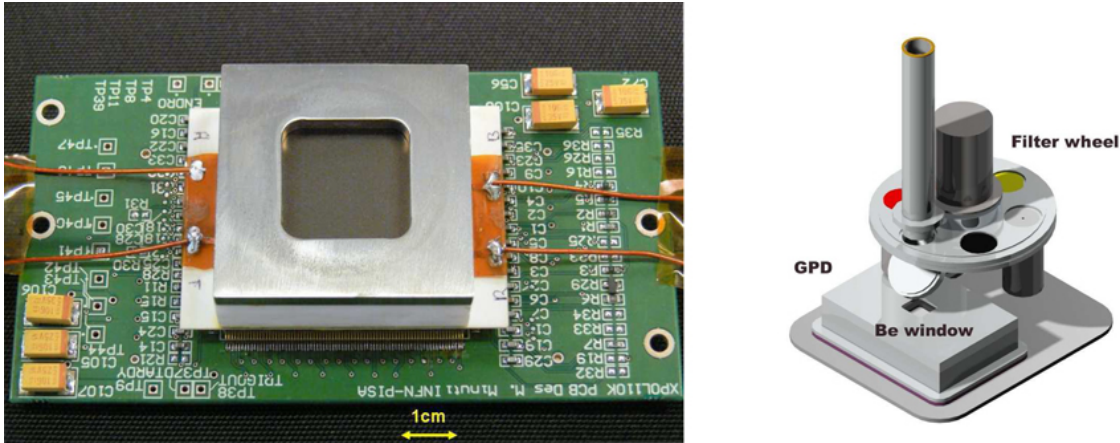


Figure 3.10: Left hand image shows a photograph of an XPOL prototype. Left hand figure shows a schematic representation of the XPOL fully assembled. A long baffle limits the FOV of the instrument and can discriminate certain photons with an additional filter wheel. (Bellazzini et al., 2010)

High Timing Resolution Spectrometer (HTRS)

The HTRS (Figure 3.11) onboard of IXO will enable the observatory to investigate even the brightest X-ray sources in the sky. It will have a sub-millisecond time resolution of around $10 \mu\text{s}$ and a low dead time of 300 ns per event. Furthermore, it will only suffer from very low *pile-up* with estimates of around 2% for sources at 1 Crab⁶. Implementing a monolithic array of *Silicon Drift Detectors* (SDD), which are similar to the macropixels presented in Section 2.4.2, the detector array will contain 31 cells, which are not square pixels, but circular sectors of varying size, getting larger in collecting area from the inside to the outside of the sensitive area. These pixels will be illuminated out of focus, evenly distributing the incoming photons over the whole detector area, thus reducing the risk of pile-up even further. The total X-ray sensitive volume will be $4.5 \text{ cm}^2 \times 450 \mu\text{m}$. Since the detection efficiency of photons above 10 keV decreases rapidly for a bulk thickness of only $450 \mu\text{m}$, an additional 1 mm thick layer of CdTe might be added to the design. Estimated count rates are 457000 counts/s for the bulk and around 600 counts/s for the CdTe layer at fluxes of 1 Crab. The aim of the HTRS is to correctly handle count rates up to a few million counts/s, and preliminary simulations show, that fluxes up to 5 Crab should be achievable. The instrument will operate in an energy range of 0.3 - 15 keV and provide an energy resolution of around 200 eV at 6 keV (150 eV are aimed for). It will mainly be used to observe sources like transient or persistent X-ray binaries during their quiet or burst phases. (Barret et al., 2010)

A digital *Data Processing Unit* (DPU), which will be based on an FPGA⁷ design, is also foreseen for this instrument and is currently being developed at the *Institute for Astronomy and Astrophysics in Tübingen* (IAAT).

⁶A flux of 1 Crab is equivalent to $3 \cdot 10^{-8} \text{ erg/cm}^2/\text{s}$.

⁷Field Programmable Gate Array. An FPGA is an *Integrated Circuit* (IC), whose behavior can be altered depending on the context of its utilization. More specific information will be given in Section 4.2.

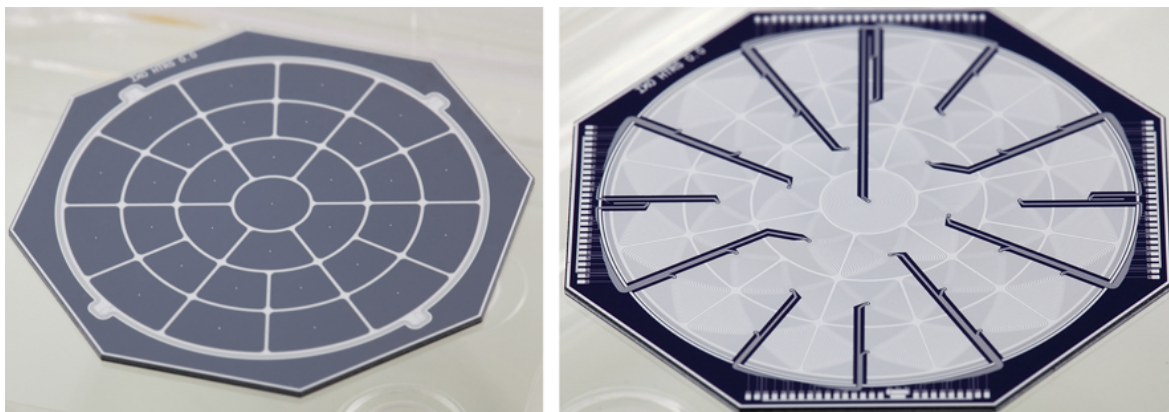


Figure 3.11: Left image shows a photograph of the Si based detection area of a dummy HTRS and the non-square pixel layout of the 31 SDDs. Right hand figure shows the corresponding backside of the detector. (NASA, 2010)

Hard X-ray Imager (HXI)

The HXI (Figure 3.12) will not be an instrument all by itself, but will be integrated in a sandwich structure together with the WFI. It is one of the key elements of IXO, since it will extend the observatory's imaging capabilities up to 40 keV. Together with IXO's supposed collecting area of 150 cm^2 at this energy, it is one of the main aspects, which distinguishes IXO from other X-ray missions of the past. The HXI will consist of a $5 \times 5 \text{ cm}$ double-sided *Cadmium Telluride* (CdTe) strip detector for the high energy photon detection. In order to shield the detector from fluorescent light and other background influences, the five sides of the detector will be surrounded by a *Bismuth Germanate* (BGO) *anti-coincidence shield*. Since the WFI's bulk material becomes increasingly transparent for photons with energies higher than 10 keV, the CdTe detector of the HXI will absorb these photons (at nearly 100% efficiency) and therefore always observe simultaneously with the WFI. Its energy resolution will be 1 keV FWHM at 30 keV and its FOV will be $8 \times 8 \text{ arcmin}$. In addition to the CdTe strip detector, two layers of *double-sided silicon strip detectors* will be mounted above the CdTe to serve as background detectors and generate an overlap between the WFI and the HXI in the band of 7 - 30 keV. (Bookbinder, 2010)

Wide-Field Imager (WFI)

The WFI is another instrument, which IXO inherited from the XEUS mission plan. It will be implemented as a Silicon-based photon detector integrated on a monolithic wafer and operate in the energy range of 0.1 - 15 keV. It will be capable of X-ray imaging with an array of 1024×1024 DEPFET-based pixels, which have a size of $100 \mu\text{m}^2$ square and allow a five-fold oversampling of the observatory's PSF. Furthermore, the large FOV of 18 arcmin will translate into a diameter of almost 10 cm of detection area in the focal plane. The WFI will have a nearly *Fano*⁸-limited⁹ energy resolution of 130 eV at 5.9 keV. Due its integration

⁸Ugo Fano (*1912, †2001) was an Italo-American physicist.

⁹The production of electron-hole pairs in a semiconductor due to the interaction with a high energy photon is a statistical process and thus ultimately limits the energy resolution of a semiconductor-based detector.

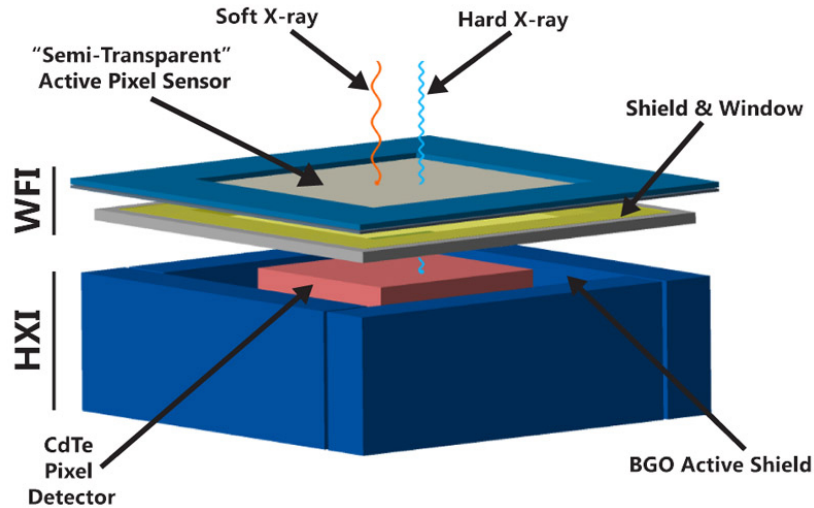


Figure 3.12: Schematic representation of the sandwich structure of the HXI together with the WFI. (NASA, 2011b)

onto the monolithic wafer, it will have a homogeneous backside entrance window, suited for backside illumination and offering a fill factor of 100%. The WFI will offer unique features, amongst them very fast readout for the entire detector area. Its readout speed of 1000 frames per second or $2\ \mu\text{s}$ per line, will not only reduce the pile-up probability for very bright X-ray sources, but also allow high timing resolution spectroscopy of variable sources with very good spatial resolution.

The layout of the WFI is somewhat complicated, but serves the purpose of allowing high readout speeds and increased safety against instrument failure. It is divided into two main hemispheres, each of which are furthermore divided into 8 sectors. Each sector will contain 512×128 pixels with two pixels being read out in parallel, hence each sector will be connected to a dedicated ASIC with two 14 bit *Analog Digital Converters* (ADC). At the moment, the type of ASIC used for this task is not decided for yet. In current prototypes, a CAMEX ASIC - which was developed by the MPE - is used for readout, but is likely to be replaced by faster ASTEROID or VELA ASICs, which will offer more functionalities, like single pixel and window mode readout. One advantage arising from the multitude of separate readout areas and ASICs is redundancy. Should one of the ASICs fail, the others are still operational and only a small portion of the original FOV is lost. (Lechner et al., 2010)

A prototype of the WFI with 64×64 DEPFET pixels at a pixel size of $75\ \mu\text{m}$ square, has already been successfully tested under laboratory conditions with operating temperatures of -50°C and evacuated surroundings by Dr. Michael Martin at IAAT. Backside illumination measurements have shown, that the prototype already reaches an excellent energy resolution of $132.8\ \text{eV}$ at $5.9\ \text{keV}$ (Mn K_α line of ^{55}Fe) for a readout speed of $2.088\ \text{ms}$ per frame (Martin, 2009). With an foreseen energy resolution of $150\ \text{eV}$ at $6.0\ \text{keV}$, it already operates within its required specifications.

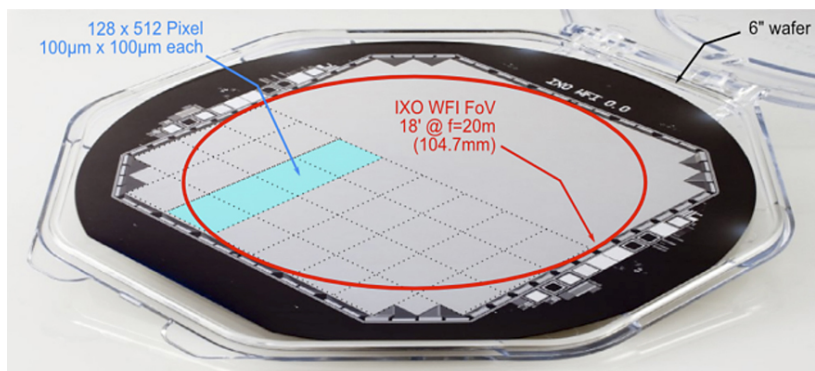


Figure 3.13: Photograph of a WFI prototype. Drawn onto the photograph is one hemisphere of the WFI design, as well as one stripe (bright blue), which is connected to one dedicated ASIC with two ADCs. The WFI is currently planned to be implemented on a 6" wafer, offering a 18 arcmin FOV at a focal length of 20 m. (de Korte, 2011)

3.2.4 Science Goals

As an intended successor to the XMM and Chandra missions, IXO will also have an updated scientific agenda. Many of these new agenda items require improved characteristics in terms of energy resolution, effective area and detectable energy bandpass. In general, IXO will aim at the observation of sources which are even fainter, than what is observable today and look even further into the history of our Universe. As a proposal to ESA's CVP IXO will focus in detail on the two questions "How did the Universe originate and what is it made off?" and "What are the fundamental physical laws of the Universe?". Observations conducted in the framework of these fundamental questions, can be divided into seven sections having their own detector requirements. Bookbinder (2010) give a very thorough summary in their activity submission and some of its aspects will be presented in the following paragraphs.

Studies of Strong Gravity For studies of strong gravitational fields and the physical processes in their vicinity, one key aspect of IXO is its large effective area of 6500 cm^2 at 6 keV photon energy. Parcels of gas in accreting flows around SMBHs have almost circular orbits and form accretion disks of high geometric and dynamic simplicity. These flows can probe the space-time configurations in their vicinity and are prime objects to test *General Relativity* (GR). GR predicts so-called arcs of neutral iron K_{α} -emissions (as described in Section 1.3.1) in the time-energy plane, thus making it necessary to have highly time-resolved observations in an energy range of 6.4 keV. The XMS will be the preferred instrument for this task, since it allows the centroiding of the emission lines.

Measuring Black Hole Spin In order to measure the spin of a BH, the effective area and energy resolution at an energy of 30 keV are essential features of the observatory. Furthermore, the polarization sensitivity, which can be achieved with the XPOL instrument, will be an important asset. Since the spin of a BH strongly depends on its growth history, measuring this parameter can provide hints on the growing mechanisms of such objects. This can be achieved by measuring broadened 6.4 keV iron lines as well as the radiation polarization from

photons reflected off the accretion disks of SMBHs. The WFI/HXI combination will enable IXO to cover an area of 0.1 - 40 keV with an adequate effective area for the 30 keV range, in order to measure the hard continuum spectrum.

Neutron Star Equation of State The neutron star *Equation Of State* (EOS) will ultimately relate mass and radii of such objects. NS have the highest matter densities in nature and physics of such environments are neither well understood, nor can they be reproduced in terrestrial laboratories. Consequently, the measurement of radii and masses of Neutron Stars is a key element in the research of matter under extreme conditions. IXO will conduct such measurements for approximately ten known NS by measuring energy dependent pulsations, which are presented during *thermonuclear X-ray bursts* from fast spinning NS in LMXB systems. The high count rates of the HTRS, as well as its good spectral resolution, will therefore be the most important tools for this study.

Growth of Supermassive Black Holes SMBHs at the center of AGN are critical components for the formation and evolution of these large scale structures. Such sources are very far away (at high red-shifts) and can only be investigated with large effective areas, since their corresponding photon flux is very low ($3 \cdot 10^{-17} \frac{\text{erg}}{\text{cm}^2\text{s}}$). With an effective area of 30000 cm² at 1.25 keV, IXO will be able to observe embedded SMBH of $10^7 - 10^9 M_{sun}$ even at high red-shifts of $z \sim 8$. Due to its operational energy range, spectral capabilities and large FOV, the WFI/HXI instrument will be the instrument of choice for these studies.

Evolution of Galaxy Clusters and Feedback The formation of galaxies and large scale galaxy clusters is strongly dependent on the physical and chemical properties of the intergalactic medium. The IGM on the other hand is strongly influenced by galactic outflows of energy and heavy elements, which is called *feedback* into the ISM. So far, only the IGM of nearby clusters at red-shifts of $z \sim 0.5$ has been investigated. IXO however, will enable studies of galactic clusters up to red-shifts of $z \sim 2$, due to its large collecting area at 1.25 keV. The high resolving power of the XMS instrument will measure velocity structures of galaxy clusters and determine their state of evolution. With a large FOV it will be possible to observe the feedback from cluster cores, as well as metallicity and the dynamics of clusters simultaneously, thus allowing the study of their mutual connection.

Cosmology In cosmology, the study of large scale structures like galaxies is fundamental for the understanding of the past and the future of the Universe. Especially the evolution of the *mass function* of galaxies and their respective *distance-to-red-shift relationship* can place constraints on cosmological parameters and shed light on the role, which dark energy plays in cosmological processes. The energy resolution and the large FOV of IXO will help to investigate these aspects. With the XMS instrument, highly red-shifted K_{α} iron lines of about 1000 galaxy clusters at red-shifts $z \sim 10$ will be measured with resolving powers of $E/\Delta E = 150 - 300$. Also, sky backgrounds near these galaxy clusters need to be measured, thus making it necessary to observe large FOVs.

Cosmic Web of Baryons Recent astronomical studies have shown, that only part of the total mass of the Universe exists in the form of *baryonic matter*, while the other part is provided

Table 3.1: Table of the most important planned observations for IXO and the corresponding expected flux rates and energy resolution requirements. Furthermore, the primary and secondary instruments used for the conduction of these measurements are listed.

Science topic	Typ. flux [erg/cm ² /s]	Bandpass [keV]	Energy res. requirement	Instruments
Strong Gravity	$5 \cdot 10^{-11}$	1 - 40	2.5 eV @ 6 keV	XMS (WFI/HXI)
SMBH spins	10^{-12}	1 - 40	1 keV @ 30 keV	WFI/HXI (XMS)
	$5 \cdot 10^{-11}$	2 - 10	1.2 keV @ 6 keV	XPOL
NS EoS	10^{-8}	0.3 - 10	150 eV @ 0.3-6 keV	HTRS
SMBH growth	$3 \cdot 10^{-17}$	0.3 - 2	150 eV @ 1 keV	WFI/HXI (XMS)
Clusters	10^{-13}	0.3 - 40	2.5 eV @ 6 keV	XMS (WFI/HXI)
Cosmology	$5 \cdot 10^{-14}$	0.3 - 7	10 eV @ 6 keV	XMS (WFI/HXI)
Web of Baryons	10^{-11}	0.3 - 1	0.1 eV @ 0.3 keV	XGS (XMS)

by an unknown material, called dark matter and is currently investigated by scientists of various fields. Furthermore, in many galaxies and even the Milky Way, the predicted relation of baryonic to non-baryonic matter by cosmic models cannot be observed. In fact, more than two thirds are missing in respective objects, thus making it necessary to explore new theories on this topic. One possible scenario is the existence of a *cosmic web of baryons*, in which the missing baryons exist as a thin, gaseous web throughout the Universe at a temperature of around $0.3 - 10 \cdot 10^6$ K. With its energy resolution, IXO will try to verify the existence of such a web, as well as the possibility of its enrichment by *galactic super-winds*. Key observations will conduct measurements of the equivalent width of He- and H-like lines of Oxygen, Nitrogen and Carbon against the continuum of bright background AGN. These elements should cause *absorption lines* in the recorded emission spectra of the AGNs and provide information about intermediate gaseous structures. The needed resolving power of $R = 3000$ in the 0.3 - 1 keV band can be achieved by the XGS instrument.

Table 3.1 shows an excerpt from a table in Bookbinder (2010) and sums up the key observational tasks of IXO and the respective primary and secondary instrument of choice.

3.3 L2 Orbit and Bandwidth Issues

As already mentioned, IXO will be brought into a *Lissajous*¹⁰-orbit around the Lagrangian point L2¹¹, which is located at a distance of 1.5 million kilometers outside of Earth's orbit around the Sun. The reasons for choosing L2 as a center point for IXO's orbit are manifold. The benign gravity gradient at this location makes it possible to aim IXO at different sources and keep it at roughly constant distance from Earth throughout the whole year, by conduct-

¹⁰Jules Antoine Lissajous (*1822, †1880) was a French physicist and is most-commonly known for his construction of Lissajous-figures as a superposition of linear oscillations.

¹¹Lagrangian points are special points in the reduced three body problem, where the force exerted on a third body of negligible mass equals zero, due to the combined gravitational pull of the main bodies and the centrifugal force resulting from its orbital motion around the center of mass. Objects located in Lagrangian points do not change their position relative to the two main bodies.

ing only small station-keeping maneuvers. Also, thermal influences of Sun and Earth are minimal at this place, making it easier to maintain constant temperatures of IXO's scientific instruments at a constant usage of consumables. Radiation pressure caused by the Solar wind will exert a torque on IXO's large Solar collectors and therefore constantly alter its direction. By moving the observatory far away from the Sun and Earth, this influence will be greatly reduced. The orbit itself will have a diameter of 800000 km and will be completed roughly every six months. Due to the geometry of this configuration, no eclipses will occur during IXO's lifetime, thus enabling observations of all parts of the sky for an extended period of time. (STSI, 2011)

All these advantages come with one major disadvantage though. Due to its large distance from Earth, transferring measured data from the satellite to the ground laboratories becomes an issue of great importance. In case of the WFI, the corresponding bandwidth reserved by IXO will be approximately 450 kbit/s (Barcons et al., 2011). It was already noted, that the WFI will consist of approximately one million pixels, each of which will carry a 14-bit energy information and will be read out 1000 times per second, thus creating gigabytes of data per second. All pixels could in principle contain valid scientific information, making it necessary to analyze every single one of them. The following calculation gives an estimate of the expected data-rate per second for the WFI:

$$\frac{\text{data}}{\text{s}} = 1000 \frac{\text{frames}}{\text{s}} \cdot (1024)^2 \text{ Pixel} \cdot 14 \frac{\text{Bit}}{\text{Pixel}} = 1.709 \frac{\text{Gbyte}}{\text{s}} \quad (3.1)$$

It has to be stressed, that this large data-rate is solely due to observations of the WFI and with the bandwidth of 450 kbit/s, will generate approximately nine hours of download time per second observation. Consequently, large data storage systems would be necessary onboard of IXO, a situation that is not feasible due to many reasons, such as weight and radiation resistance of memory, just to mention a few.

Going back to Section 3.2.1 it was noted, that IXO will mainly look at very faint objects. Consequently, most of the time, pixels will not carry important scientific information as the photon flux rates of these objects are very low (compare Table 3.1). Transferring and storing all recorded data would thus result in a utilization of bandwidth for the transmission of invaluable information (pixels would mostly contain noise and background information) to the ground. In order to deal with this circumstance, discarding pixels without important information onboard of IXO, can be a very effective way to limit the amount of data, which has to be transferred to Earth. The EPP, which will be described in Chapter 5 represents the first stage of onboard, hardware-based realtime analysis of pixel data from the WFI. Each pixel's energy information can be flagged as valid or invalid and only be transferred to the ground if needed, thus reducing data rates by many orders of magnitude.

Since the sensitive energy range for the HTRS instruments is almost the same as for the WFI, information from the *IXO Yellow Book* can be taken in order to create a first crude estimate of the expected count-rates for the WFI. At a photon-flux of 1 Crab, the HTRS expects 170000 counts/second in an energy range of 0.3 - 15 keV (Barcons et al., 2011). Taking a source at 10 mCrab for example, this will translate to 1700 counts/second for the WFI. Additional to photons originating from the source, background events also have to be considered. Recent *Geant4*¹² simulations by Hauf et al. (2009) have shown, that the background rate for an

¹²Geant4 stands for GEometry ANd Tracking and is the fourth version of a commonly used platform for the simulation of the passage of particles through matter, based on Monte Carlo methods.

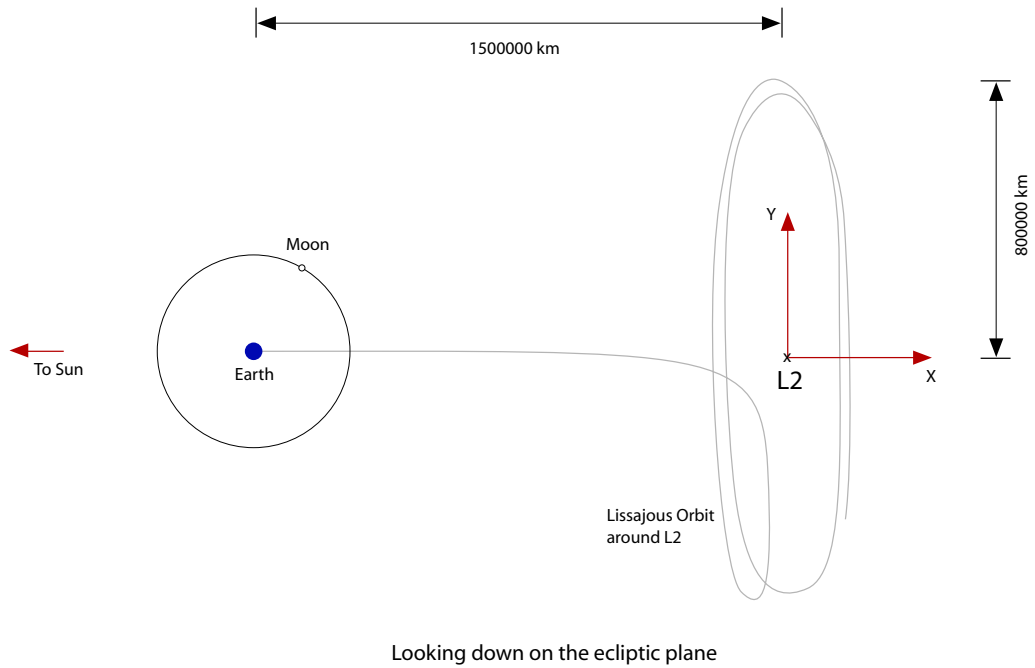


Figure 3.14: Schematic representation of the trajectory IXO will follow. Reaching L2, IXO will go on an orbit around the Lagrangian point with a radius of 800000 km. (STSI, 2011)

energy range of 0.1 to 15 keV can be approximated as $15 \cdot 10^{-3}/\text{cm}^2/\text{s}$. Taking the detector area of the WFI into account, a total of 1702 events per second are expected for the WFI. In a worst-case scenario, each event will create a *quadruple pixel pattern* on the detector, thus causing an effective data amount of 435712 bits (64-bit information per pixel from the EPP). Compared to the raw-data rate of 1.709 Gbyte/s, the resulting data-rate will be reduced by 99.997%.

4 Designing Hardware

Ever since the invention of the transistor by Schockley¹, Brattain² and Bardeen³ at the Bell Labs in 1948 (Bardeen et al., 1948), it has become possible to build electronics, which are based on discrete voltage levels. Together with the *Boolean*⁴ *Algebra*, these discrete electronics, also called *digital electronics*, made it possible to reproduce electric circuits to have the exact same characteristics as their blueprint without any calibration and to predict their behavior prior to their manufacturing. Nowadays, digital electronics can be found in almost every electric device. They have increased in complexity from the beginnings, while their lifetimes and product-cycles have shrunk almost at the same rate. For astrophysical applications and the control and operation of modern detector systems, digital electronics are an essential asset. With their help, it has become possible to prepare data for further processing and analysis on computers, thus enabling scientists to handle giga- or even terabytes of data and conduct statistically relevant research. This chapter deals with the development of digital electronic systems and presents a way to design and test them in the framework of *Field Programmable Gate Arrays* (FPGA) and the *Very High Speed Integrated Circuit Description Language* (VHDL).

4.1 Important Digital Components

4.1.1 Integrated Circuit (IC)

The term *Integrated Circuit* (IC) describes an electric circuit, which is implemented onto a thin semiconductor substrate by the diffusion or injection of trace elements, acting as electronic components, just on a much smaller scale. ICs are often called *chips* or *microchips* and all necessary electronic parts, as well as their interconnection, are located on the substrate. Due to their small size, ICs have very short switching times, low power consumption and have driven the miniaturization of most electronics, since their invention. Their range of functionality can reach from the simplest logic operations, such as AND and OR gates, up to complex assemblies of millions of transistors for modern day microprocessors (CPUs). However, once an IC has been created, it cannot be changed anymore. As a consequence, there are many commercially available ICs, which conduct standard operations and can be interconnected and used in a variety of electric devices. (Seifart and Beikirch, 1998)

¹William Bradford Shockley (*1910, †1989) was a US physicist and recipient of the Nobel Prize in physics in 1956, together with Brattain and Bardeen for their discovery of the transistor effect.

²Walter Houser Brattain (*1902, †1987) was a US physicist and recipient of the Nobel prize in 1956, together with Schockley and Bardeen.

³John Bardeen (*1908, †1991) was a US physicist and recipient of the Nobel Prize in physics in 1956, together with Schockley and Brattain. He was also awarded a second Nobel prize in physics in 1972 for his contributions to the fundamental theory of superconductivity.

⁴George Boole (*1815, †1864) was a British mathematician logician and philosopher. He is the inventor of the first algebra based logic analysis.

4.1.2 Application-Specific Integrated Circuit (ASIC)

An *Application-Specific Integrated Circuit* (ASIC) is a typically complex IC, which was designed for one specific operation. It can contain millions of transistors, house memory and even microprocessors on its substrate and is often referred to as a *system on a chip*. The production of ASICs is very expensive, but design errors can be avoided by using *Hardware Description Languages* (HDL) and *Uncommitted Logic Arrays* (ULA). ULAs are arrays of standard logic gates, which are grouped in so-called *standard cells*. The position and distance of these cells is integrated and can therefore not be changed anymore. Their connections on the other hand, can be controlled by adding a metal-layer onto the substrate, which will interconnect the cells in a way, which will reach desired functionality and optimum performance. The design of the metal-layer is called *Place And Route* (PAR) and will also play an important role, when switching from ULAs to FPGAs. (Seifart and Beikirch, 1998)

4.2 Field Programmable Gate Arrays (FPGAs)

FPGAs are special representatives of ASICs and comparable to ULAs. For FLASH⁵ or EPROM⁶ based FPGAs, the final step - creating the metal layer to imprint functionality - does not have to be conducted at the hardware level. Instead, the information about the connections in between standard cells is stored as data in so-called *Lookup-Tables* (LUT) in the integrated FLASH or EPROM memories of the FPGA and can be rewritten up to a few thousand times until degradation renders it unusable. Compared to ASICs, FPGAs are usually inferior in terms of power consumption and switching times. In terms of development however, they are more flexible and allow corrections of the design, even if it has been implemented already, thus reducing the risk of creating an erroneous ASIC, which has to be redesigned. As a result, it is fairly common to utilize the advantages of both devices and manufacture ASICs with functionalities, which have previously been tested with the help of FPGAs.

One major aspect, which distinguishes different FPGAs, is the number of *logic cells* they contain. Their amount will ultimately decide how many tasks can be conducted by the FPGA and what grade of complexity an FPGA-based electronic can have. It will furthermore decide how fast an FPGA-based device will be able to operate, since the shortest distances between logic cells can be realized, if whole blocks of cells are available for usage and not obstructed by other parts of the design.

Together with their parallel working capabilities, FPGA have become very popular in fields where the distribution of tasks on different working threads can result in increased operation speed, such as digital video and audio editing. With the current-paradigm shift in the microprocessor industry, where manufacturers are switching from ever increasing clock frequencies to an increase in the number of processing cores, it becomes clear, that parallelism is also of interest for commercial computing applications. It is therefore likely, that the importance of FPGAs for the design process of hardware and probably even software will increase considerably in the future.

⁵Memory which can be written or erased electronically.

⁶Erasable Programmable Read Only Memory.

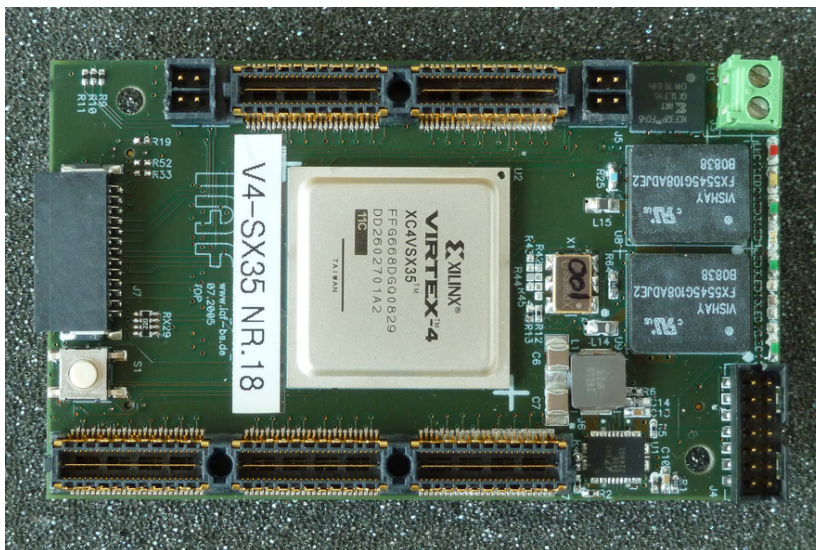


Figure 4.1: Photograph of a Xilinx Virtex-4 SX 35 mounted on a IAF carrier board.

4.2.1 The Xilinx Virtex-4 SX 35 FPGA

For the first test runs of the EPP, a *Xilinx Virtex-4 SX 35* FPGA was used as target hardware. The Virtex-4 series consists of many different types of FPGAs, which mainly differ in the number of available logic cells, *slices* and RAM resources. The Xilinx Virtex-4 SX 35 contains an array of 96 x 40 *Configurable Logic Blocks* (CLB), which furthermore consist of four slices each. Each slice on the other hand is a group of two function generators, two storage elements, arithmetic logic gates, large multiplexers and a fast carry look-ahead chain. The function generators are implemented as 4-lookup tables, which are LUTs with four input signals and one output signal. By default, two of the four available slices in a CLB are configured as 16-bit *shift registers* or as 16-bit *distributed RAM*. Utilizing shift registers or distributed RAM instead of *block RAM* resources, will therefore immediately affect the available CLBs and the speed of the design. The two storage elements are either edge-triggered D-type flip-flops or level-sensitive latches. As a result of these numbers, the Xilinx Virtex-4 SX 35 contains a total of 15360 slices, 34560 logic cells and 30720 CLB flip-flops, which can be used in a VHDL design. Concerning memory, the FPGA can offer a total of 240 kB of distributed RAM and approximately 3456 kb of block RAM. It offers 448 I/O ports, distributed on eleven I/O banks with a digitally controlled impedance. Aside from regular slices, the FPGA also offers 192 *XtremeDSP* slices, each of which contains a dedicated 18 x 18-bit 2's complement signed multiplier, an adder logic and a 48-bit accumulator.

One reason for the selection of this specific FPGA as target hardware for the EPP was, that the same model also exists in a radiation hard version. Especially for space-based operation of FPGAs, this is an important quality. Reasons for this will be given in Section 4.5.

4.3 VHDL

VHDL is a hardware-description language, which is used to plan and design complex digital electronic systems. It can be compared to a common procedural programming language like *C*

or *FORTRAN*, but adds the functionality of so-called *processes*. Processes control operations, which are conducted in parallel, and which are triggered by changing *inputs*, such as a *clock signal*. Since processes are one crucial aspect of VHDL and FPGAs, further information about them will be given in Section 4.3.1. In VHDL, digital electronic systems are represented by *models*. A VHDL model is independent of the electronic parts, that will later be used to implement the hardware and is interchangeable between developers using different design platforms or electronics. In general, a VHDL model or *module* consists of two parts, called the *entity* and the *architecture*. (Ashenden, 2001)

Entity The entity of a VHDL model defines its interface to the outside, where the described electronic could be (and in most cases will be) interconnected with other electronic devices. It contains all signal ports, such as inputs and outputs, as well as their corresponding type. Input signals are used internally to perform operations, while results of these operations are allocated to the respective output ports and can be used as input values for other design components. In a way, compared to real hardware, it can be thought of as the socket of an electrical component.

Architecture The architecture of a design contains a *structural* or *behavioral description* of the operations, which will be performed by the described electronic. It will utilize all signals received from the input ports in order to perform various operations, which can be conducted by logical manipulations of signals. Signals are similar to variables, which also exist in VHDL, but are not assigned instantaneously in a sequential manner. Instead, all signals within one process are allocated in parallel and can only be read in discrete time-steps or clock cycles. It has to be added, that one VHDL model can contain more than one architecture. This is essentially useful if different design ideas, which offer the same final functionality, are tested against each other. In this case, VHDL allows to pick a *configuration*, which will map one of the existing architectures to the entity of the design.

If a behavioral description is chosen for the architecture, the function of the module is described in an abstract way with the help of processes, which control the values on the entity's ports.

If a structural description of the architecture is chosen, it will solely consist of a description of how subsystems (like latches, gates and other components) are interconnected.

In many cases, an architecture will neither be structural nor behavioral, but mixed. A structural part will instantiate components, which are needed to perform certain operations in a module, while the behavioral part will describe, how signals are assigned to these components and how their respective outputs are routed to the output of the module.

4.3.1 Processes

Processes are the central structures of each VHDL design and control the behavior of a module. They are located within the architecture and operate on signals, that have been read from the entity and stored in registers. In general, a process will contain a sequential list of statements and signal allocations, which will all be executed once the process has been started. In order to trigger this start, it will have a *sensitivity list* in most cases. This list will contain signals, which are read from inputs of the module and can vary with time. Any-

time one of these signals changes, the process is triggered and will conclude all operations it contains before waiting for the next signal change. Usually architectures contain multiple processes, which are started by the same trigger signal. As a consequence, each input signal in the module can only be manipulated by one specific process, in order to prevent collisions, that could arise otherwise.

In most cases, the trigger signal is a clock signal, starting processes with a constant period. The minimum length of this period is strongly dependent on the number of tasks conducted by one process, since it is essential in digital electronics to wait for all processes to be finished before starting a new cycle. Consequently, distributing all tasks a module has to conduct onto several, clock-triggered processes, can be a way of effectively increasing working frequencies of digital electronics. In principle, this can be thought of as an assembly line. The processes of a design are represented by workers conducting different tasks at the same station in the assembly. The assembly line can only move forward and distribute parts - which represent signals - to other stations, if all workers of one station are done with their respective work. The speed of the slowest worker (or process) therefore defines the speed of the whole assembly line and thus the electronic.

The utilization of multiple processes in one module is one of the key-elements in the development of the EPP. The ability to have tasks, which are conducted in parallel, allows to design highly effective data analysis hardware components. More information about these components and their respective processes will be given in Chapter 5.

4.3.2 Typical Structure of a VHDL Design

It was already mentioned, that most VHDL designs will be mixed designs, meaning they will contain elements of structural and behavioral descriptions. Figure 4.2 shows the typical layout of a VHDL design. First of all, the header contains information about libraries, which will be used in the design. Many definitions like operations, which can be performed on certain data types are stored in these libraries and are used by the compiler to check for semantic errors in the source code. Following these values is the definition of the entity of the module. Here, all input and output ports are declared, as well as the signal type they carry. Also, default values for output signals can be assigned in this block. After the entity, the architecture of the design is defined. The header part of the architecture should contain all internal global signals, which are used for operations within the module and can later be assigned to output ports of the entity (but do not have to). The types of these signals are also set in this block, as well as their default value for the initialization of the unit. Following the signals, there is a list of component declarations for the module and the entity of each component, which will be used in the module, is defined. The header of the architecture is finished once the keyword `begin` is written. Here, the body of the architecture begins. Its first part contains instances of components, whose entities were defined in the header and will be connected to signals (which have also been declared in the header) by a so-called *port map*. Not all ports of a component entity have to be connected, but can be left unconnected if the keyword `OPEN` is used, instead of an existing signal name. Once all components are instantiated and their port maps have been assigned, the structural part is finished and the behavioral part follows. Here, processes, which control operations on the signals within the unit, are located. The last stage in a VHDL design file contains information about the connection of certain registers or input

ports to the output ports of the entity. However, connections are only placed in this part of the design, if the update of output ports of the entity does not have to be clock synchronous, but can be static.

4.4 Designing Hardware

In general, the process of designing hardware with the help of HDLs is also called *synthesis*. Many functionalities can be described with the help of an HDL, but not all functionalities can be implemented in real hardware, mostly due to timing issues. A typical hardware design can be separated into four steps, which are also visualized in the flowchart of Figure 4.3.

Description via HDLs The first step of each hardware design is the description via an HDL. Here, the unit is described as a whole or as an assembly of smaller *components*. In the latter case, the most functional structure, which will implement smaller designs as modules, is called the *top-level* of the design. One common way of splitting large designs into smaller parts is by successive reduction of complexity of the unit. If it has to perform a number of tasks, each task will be accomplished by a single component, which will furthermore implement basic structures, such as registers, counters and so on. If the functionality of a component can be mapped onto these so-called *primitives*, the *Xilinx Synthesis Tool* (ST) will do so automatically.

Once the design is finished, it will be verified by a compiler, which will check syntax and semantics for errors. Afterwards its behavior can be visualized with the help of HDL simulators like *Xilinx ISim* or *Modelsim* and the design can be checked for timing errors and functionality issues. Each signal within the design is visible as a value vs. time graph and registers or counters are represented by their respective value for each time-step, which means, that for every clock cycle, the designer can check whether they contain the correct values or trigger the correct signal responses in other parts of the module.

Extensive software simulation of hardware is usually accomplished with the utilization of *test-benches*. A test-bench acts as a top-level design, which instantiates the *Unit Under Test* (UUT) as a component. It can alter the units input signals automatically via processes or manually in precisely user-defined time-steps. Test-benches can usually not be implemented as real hardware, but serve the purpose of testing HDL modules in a realistic way. In case of the EPP design presented in this thesis, each component, as well as the top-level design, was tested in a test-bench environment.

Synthesis / Technology Mapping After the design has been simulated and shows correct functionality, it will be synthesized by a ST. The ST itself is dependent on the type of hardware the design will be implemented on and therefore differs for various manufacturers of FPGAs, such as Xilinx, *Altera* or *Actel*. Due to this specialization, the ST uses the information of the specific implementation hardware and maps the design onto its available resources. As described in Paragraph "**Description via HDL**", the synthesis tool will try to utilize primitives for the desired operations and closely analyze the HDL code. Depending on the complexity of the design and the processing speed of the computer used for synthesis, the ST will need minutes or even hours to complete this analysis, which emphasizes the necessity of thorough test-bench simulations, in order to find design errors up front.

<pre>library IEEE; use IEEE.std_logic_1164.all;</pre>	Header
<pre>entity UNIT is port (CLK : in std_logic; PORT_A : in integer range 0 to 7; ... PORT_Z : out std_logic := '0') end UNIT;</pre>	Entity
<pre>architecture FUNCTION of UNIT is -- signals signal SIGNAL_A : std_logic_vector(7 downto 0) := "0011000"; signal SIGNAL_B : integer range 0 to 7 := 0; ... signal SIGNAL_Z : std_logic; -- components component compA port (PORT_1 : in std_logic; ... PORT_n : out std_logic); end component;</pre>	Architecture Header
<pre>begin instanceOfComponent: compA port map (PORT_1 => SIGNAL_B, PORT_2 => OPEN, ...);</pre>	Architecture Body structural
<pre>someProcess: process (CLK) begin if rising_edge(CLK) then SIGNAL_A <= "1001101"; ... if SIGNAL_B < 8 then SIGNAL_B <= SIGNAL_B + 1; else SIGNAL_B <= 0; end if; PORT_A <= SIGNAL_B; end if; end process;</pre> <pre>end;</pre>	behavioral

Figure 4.2: Typical Layout of a VHDL file.

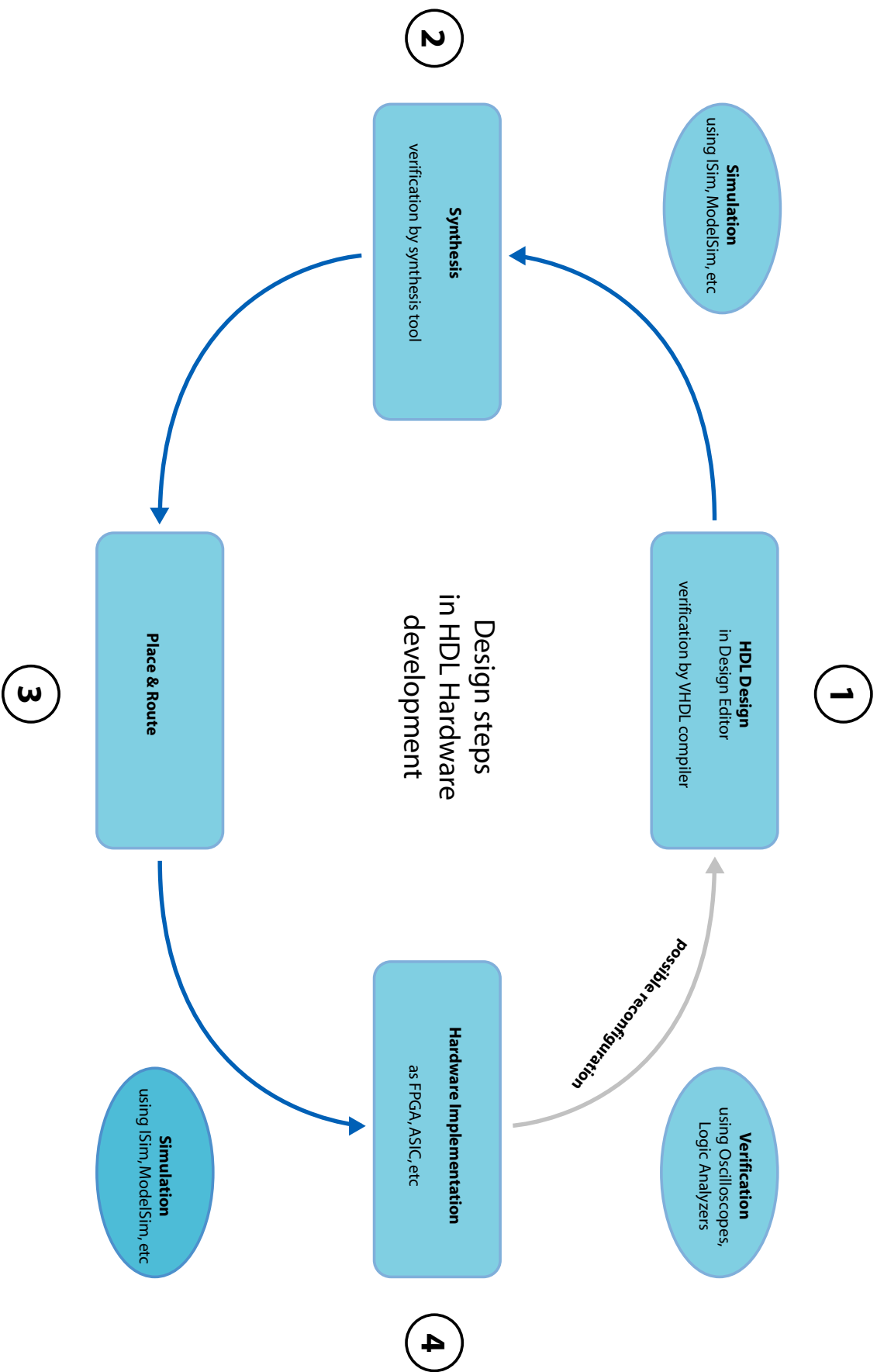


Figure 4.3: Visual representation of the four most important design steps in HDL design. In case of FPGAs and other reconfigurable ICs, steps 1 through 4 can be completed multiple times, until the desired performance and functionality of the hardware is achieved.

Place and Route During synthesis, the ST will only check, if a mapping of the units functionality onto the selected hardware is possible. Once this has been verified, the placement and connection of each component with the target hardware is conducted either automatically or manually. In case of Xilinx FPGAs, the company offers an elaborate routing tool, which tries to occupy as little of the available resources as possible. Also, it will identify, if resources for separate operations may be shared and furthermore reduce the unnecessary usage of CLBs. Aside from this optimization, the PAR phase of the design will try to utilize short interconnections between components, in order to effectively reduce long signal runtimes, which can cause waiting times and slow down the maximum clock frequency of the design. Lastly, power-consumption of the target hardware and connected heat-dissipation can play an important role and will be optimized in this step, prior to the final implementation. Once the PAR is finished, it is possible to run another software simulation, considering the real placement of components in the FPGA, which allows to utilize a more realistic timing scenario. This process is also called *back annotated gate level simulation*.

Hardware Implementation Finally, once the design has been simulated, synthesized and routed, it can be implemented in the target hardware. In case of Xilinx FPGAs, the development environment will generate a bit-file, which can be loaded into the *Programmable Read Only Memory* (PROM) of the FPGA. At every startup, the information of the PROM is transferred into the FPGA and programs the device for operation. Also, default values for RAM and constant registers are transferred and become available for readout once the FPGA has been initialized.

At the end of this chain it is also possible, to implement the design as an ASIC. However, once the ASIC is produced, developers cannot go back in the chain and reconfigure functionality aspects. In the case of FPGAs, steps 1-3 can be conducted multiple times, until an optimum and error-free performance is reached.

At this stage, the verification of implemented hardware is conducted with the help of testing boards (also called hardware test-benches), which provide a variety of pins, LEDs and other input/output ports for measuring signal timings and values. With the help of oscilloscopes and logic analyzers it is possible to investigate signals, which consist of multiple bits, on a time-scale of nanoseconds. This time-scale is usually sufficient, since most FPGA designs run at clock frequencies of 100 or 200 MHz (with clock periods of 10 ns or 5 ns respectively).

4.5 FPGAs for Space-related Operation

It was stated already, that the design of hardware is a very cost-intensive process, especially in the case of ASICs. Furthermore, FPGAs operate at clock frequencies of 100 - 200 MHz, which is way below the clock frequencies of modern day CPUs, operating at speeds of 2 - 3 GHz. Considering the cost for oscilloscopes, logic analyzers and other electronic equipment, which is needed for the verification of an electronic design, the cost of software programming and testing will be considerably lower. As a consequence, CPUs and software might seem superior to FPGAs and ASICs, but are outperformed by them in many disciplines, which are important for space-based science applications.

First of all, due to the ever decreasing transistor size of CPUs, they would degrade very rapidly in typical space radiation environments. With a size of 32 nm in the case of the *Intel Core*

i7 series for example, millions of transistors can be placed on one die. If highly energetic particles, such as charged protons or electrons struck the CPU, they would likely damage or even destroy one or more transistors at once, thus rendering the CPU inoperative after a short period of time. Many FPGAs are fabricated with the same technology, but also exist in *radiation tolerant* or *radiation hard* versions, while most CPUs do not. Other types of FPGAs like Actel *AntiFuse* FPGAs are even intrinsically radiation hard. As a result, FPGAs outperform regular CPUs in terms of radiation tolerance and hardness.

A second reason for choosing the low frequency FPGAs instead of CPUs is their power consumption. Resources on a spacecraft are sparse and one design goal for space-qualified hardware is low power consumption. For the WFI onboard of IXO, the mission plan foresees a power consumption of the whole instrument (including all electronics) of 348 W with contingency (Bookbinder, 2010). One Intel Core i7 CPU by itself, already consumes 130 W and therefore 37% of the total allowance, when working at full capacity (Intel Corporation, 2010). Since it is planned to implement multiple EPPs for the readout of the WFI detector stripes, using multiple CPUs would be impossible. The Xilinx Virtex-4 SX 35 FPGA on the other hand has a typical power consumption of 4 - 5 W, when fully implemented with an HDL design and therefore a factor of 26 less.

Closely connected to the power consumption of these devices is their temperature and heat dissipation. While CPUs can easily reach temperatures of 60 - 70°C (Intel Corporation, 2010), FPGAs will rarely exceed temperatures of around 30 - 40°C. As a result, FPGAs can be cooled more easily and be implemented in the proximity of temperature sensitive detectors, while CPUs would cause more thermal noise and thus degrade the signal-to-noise ratio for conducted measurements.

The most important of all reasons for choosing FPGAs, is their variability of architectures. While CPUs are ASICs fixed to one single architecture, which has to be used for data handling, FPGAs can be designed to fit specific needs of the detector's readout scheme. Specific aspects of data handling can be manually optimized and while in the case of a CPU unnecessary functionalities would not be used, in an FPGA design they can be completely left out. Consequently, FPGAs can achieve higher performances for certain tasks, especially if they involve the parallel processing of several threads of data at once. In case of the WFI, the FPGA allows processing information of more than one pixel at once, therefore enabling high readout speeds for the whole pixel matrix.

5 The Event Pre-Processor

The main topic of this thesis was the design and implementation of an Event Pre-Processor for the WFI instrument onboard of IXO. Development of the EPP began in August 2010 and so far, the VHDL source code consists of more than 3000 lines. Currently, not all of the desired functionalities have been implemented in the design, but groundwork has been laid for all aspects considered by the WFI consortium. The *Xilinx ISE* development environment estimates a usage of Xilinx Virtex-4 SX 35 slices of 52% (8011 / 15360). Furthermore, 21% (6644 / 30720) of slice flip-flops are used, 44% (13770 / 30720) of 4-input LUTs, and 12% (4 / 32) of *Global Clocks* (GCLK). Even though these numbers are not final, they are within a resource usage of 50% (aside from slices, but many test-functions were implemented, which will not exist in the final version), which is needed to implement two instances of the EPP in one single FPGA.

The current design of the EPP is shown in Figure 5.1 and will be described in further detail in the following sections. Part of it is based on an earlier design of the so-called D3C EPP, that was originally created by Thomas Schanz of IAAT for the Simbol-X mission. The exact mission specifications for Simbol-X however, were a lot different from IXO, rendering a partial redesign necessary in order to adapt the electronics to the specifications of the WFI. During the redesign it became obvious, that aspects like operational speed of the involved processes represented bottlenecks, that could not be bypassed with the work that had already been done. As a consequence, new ideas and algorithms had to be implemented, in order to ensure, that the new requirements could be met by the new EPP design.

5.1 Heritage from Simbol-X

The Simbol-X mission was originally planned as a French-Italian satellite mission with German involvement in the focal plane instrumentation. Its intended launch date was 2015, but due to budgetary reasons, the mission was cancelled by the *French Space Agency* (CNES) after completion of its phase A study. Similarly to IXO, a *High Energy Detector* (HED) and a high energy resolution *Low Energy Detector* (LED) in a sandwich structure were foreseen, in order to detect photons in an energy range of 0.5 - 80 keV. In order to reach focussing powers sufficient for such high energies, Simbol-X was planned as a formation flight mission having a focal length of approximately 20 m. The LED, covering the energy range of 0.5 - 15 keV was planned to be an *Active Pixel Sensor* (APS) with a matrix of 128 x 128 DEPFET macropixels having a size of 625 μm square, and being read out at a rate of 8000 frames per second. (Lechner et al., 2008), (Martin, 2009)

In order to cope with the high data rates caused by the read-out speed, the implementation of an EPP was foreseen, in order to filter scientifically relevant events from the raw data stream of the detector. The original design of the *D3C EPP* by Thomas Schanz used a *pipeline* of multiple units, which handled the incoming data and manipulated pixels one by one in a series

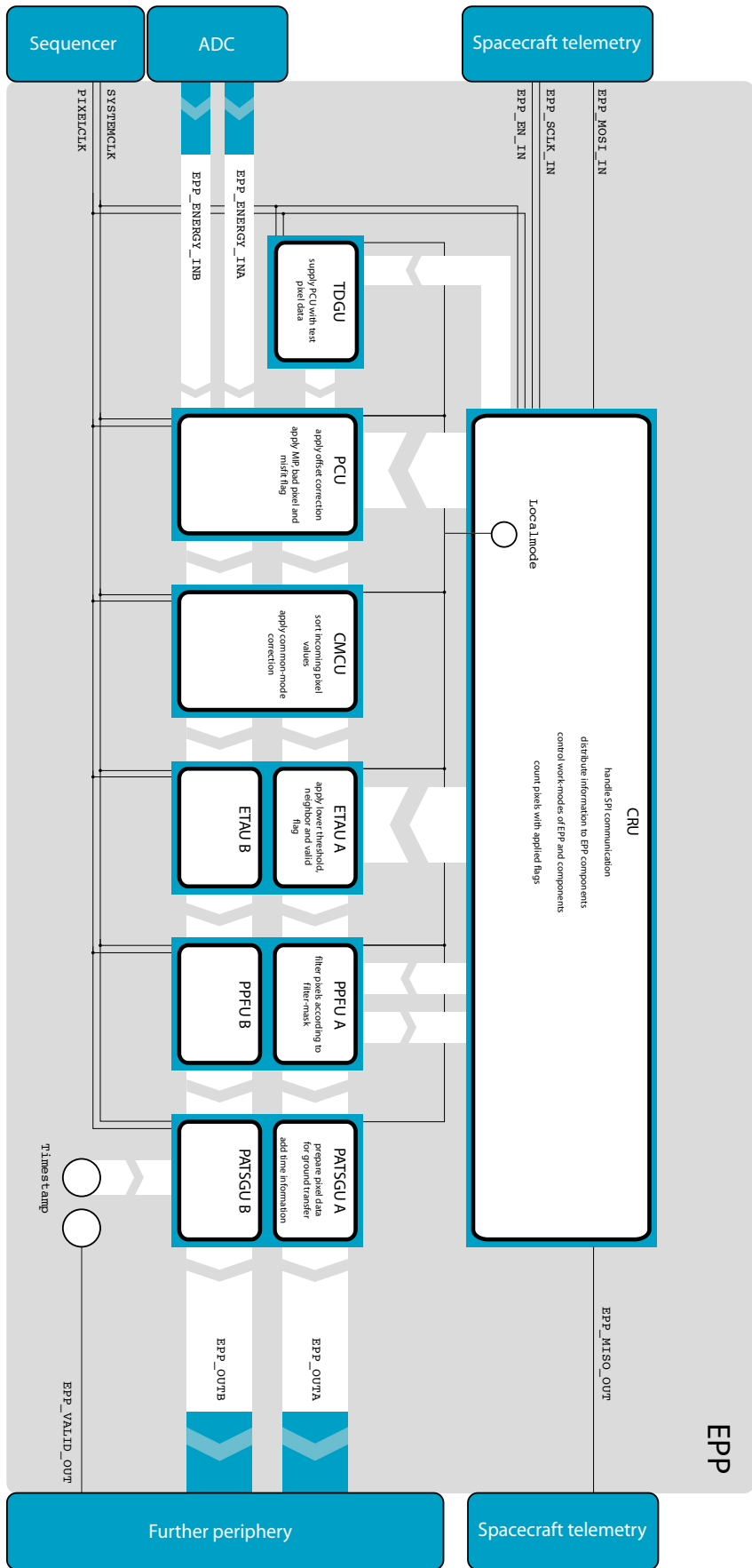


Figure 5.1: Illustration of the EPP pipeline design. The EPP entity connections are marked with their respective names and the most important signal directions are shown.

of steps. The utilization of a pipeline is an efficient way to conduct time-critical tasks, since it enables the distribution of many tasks onto different distinct stations. The idea behind this concept is to create a series of fast working operations, which together represent one time-consuming operation. Since each unit only handles one pixel at a time, this concept also allows to process many pixels simultaneously in different stages of the EPP, as a new pixel can enter the first pipeline stage, once the previous one has left it. Consequently, pixels will constantly arrive at the end of the pipeline, allowing to have constant input and output data-rates. If information is processed in such a way, it is also referred to as *realtime* data-processing.

Aside from the pipeline structure, four of the initially proposed nine D3C EPP units were taken over from the original Simbol-X design, being the *Pixel Correction Unit* (PCU), the *Common-Mode Correction Unit* (CMCU), the *Energy Threshold Analyzer Unit* (ETAU) and the *Programmable Pixel Filter Unit* (PPFU). Completing the current design of the EPP, the *Pixel Address and Time-Stamp Generator Unit* (PATSGU), the *Control and RAM unit* (CRU) and the *Test Data Generator Unit* (TDGU) were added. Further detail about the respective tasks of these units and how they were adapted to the requirements of the WFI, will be given in Sections 5.3.2 through 5.3.9.

5.2 Principle Design Constraints

Before diving into the specifics of each individual unit, this section will focus on the principle design constraints of the EPP, which are mainly derived from the science requirements of the WFI and technical aspects of the electronics the EPP will be implemented on.

5.2.1 Clock Frequencies

As already mentioned in Chapter 3, the WFI will be separated into two hemispheres which are furthermore separated into eight individual *stripes* or *sectors*. With the aimed for WFI frame-rate, each of these sectors, which contains of 512 x 128 pixels, will be read out 1000 times per second, two pixels at a time (see Figure 5.2). As a result, each instance of the EPP pipeline has to handle an amount of

$$\frac{(512 \cdot 128)}{2} \frac{\text{pixels}}{\text{frame}} \cdot 1000 \frac{\text{frames}}{\text{s}} = 32768000 \frac{\text{pixels}}{\text{s}}, \quad (5.1)$$

which limits the available time for the processing of a pixel in a specific pipeline stage to approximately 30.5 ns. This time defines the period of the so-called *pixel clock* (PIXELCLK), which is a rectangularly shaped clock signal given to the EPP by an external *sequencer*. The PIXELCLK will also trigger many processes of the EPP VHDL design, since it is the most important clock signal next to the *system clock* (SYSTEMCLK), which represents the minimum time period between two sequential process executions (refer to Section 4.3.1). Typical hardware designs, implemented on an FPGA, run at 100 MHz SYSTEMCLK frequencies, which translates to a period of 10 ns. Consequently, for this clock frequency, each EPP process can be executed three times, before a new pixel arrives in the pipeline (PIXELCLK \approx 3 · SYSTEMCLK). However, there are many operations, which have to be performed for each individual pixel, before it can be tagged as scientifically relevant or not. In general, operations like *offset corrections*, *threshold analyses* and *common-mode corrections* will take longer than

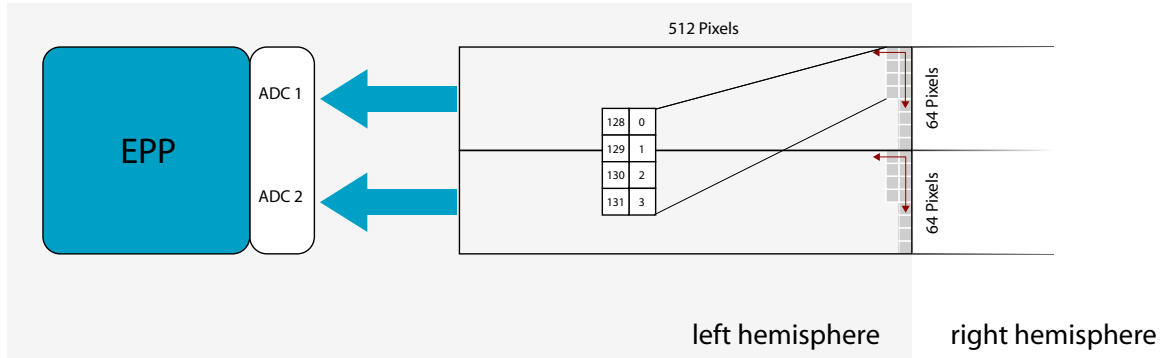


Figure 5.2: Schematic representation of the readout scheme of one sector of the WFI. Pixels are read out from top to bottom and right to left in both parts of the sector simultaneously. The respective pixel number starts at 0 and increases from top to bottom and right to left. The two ADCs convert the energy information of each pixel into digital values and pass them on to the EPP pipeline.

30.5 ns. Consequently, as already mentioned in Section 5.1, all operations are distributed onto several subunits of the EPP, which are interconnected in a pipeline. If a pixel enters the pipeline, it is manipulated by the first stage and then handed over to the next stage and so on. Each stage can operate on the pixel until the next PIXELCLK event arrives, thus enabling the EPP to apply a series of corrections and analyses.

5.2.2 Clock Synchrony

The pipeline itself is synchronized to the external SYSTEMCLK signal, even though most processes are triggered by the PIXELCLK coming from the sequencer. In theory, these two clock signals should be synchronous, but in practical applications, an effect called *jitter* can destroy this synchrony. Jitter describes the deviation of digital signals in terms of amplitude, phase timing, or the width of the signal pulse and is mainly due to electromagnetic interference or crosstalk with other signals in the proximity of the corresponding signal line. Since our electronics are synchronized to the SYSTEMCLK signal, we need a process that can notice the rising-edge of the PIXELCLK signal, even if both signals do not have rising-edges at the exact same time. The solution to this problem is to buffer the incoming PIXELCLK signal at each rising-edge of the SYSTEMCLK. This is done in a process called `setOldClock`, which is implemented in every unit. Two signals, called `PIXELCLK_INT` and `PIXELCLK_INT_OLD` buffer the incoming PIXELCLK signal for time-steps $n - 1$ and n respectively. If there is a change in the PIXELCLK amplitude, the process will reach a configuration where `PIXELCLK_INT = '1'` and `PIXELCLK_INT_OLD = '0'`, thus making it possible to recognize a rising-edge of PIXELCLK and trigger the further operation of processes in the module.

5.2.3 Signal Buffering

Due to the high frame-rate and the fast PIXELCLK, every unit of the EPP has to manipulate rapidly changing contents of internal registers. In order not to manipulate two different registers in one pipeline stage during one PIXELCLK cycle, reading from the input and writing the output are also synchronized to the PIXELCLK signal. For the manipulation itself, each

unit buffers incoming information in registers and thus works with a "copy" of the input signal, which can be compared to a call-by-value operation. This is especially useful, if incoming values from a RAM are read. RAMs are typically very slow and need two SYSTEMCLKs after being addressed to provide their corresponding memory value. If a current RAM value is buffered at the beginning of an operation, the RAM itself can immediately be addressed for another value, which will be available once the next pixel enters the unit. While the RAM address signal and its output are changed, it is still possible to work with the old RAM value for the current pixel, since it was buffered at the beginning of the PIXELCLK cycle.

5.2.4 Workmodes of the EPP

Global Workmode

In order to control the function of the EPP, a so-called *Global Mode Register* (GMR) was implemented in the CRU. It consists of four bits and stores information about the current working mode of the whole unit. So far, four different cases exist, which are implemented as a *Finite State Machine* (FSM) in the top-level of the EPP.

"0000" - stop If the EPP is in stop-mode, the process `setOldClk` is not triggered, and therefore no other processes will be notified about rising-edges of the PIXELCLK signal. As a result, the EPP will not read any values from its input, nor will it update its output with current values. Also, the EPP pipeline will not advance, which means, that processes, which are counting incoming pixels, will remain at the same count value, thus pausing the EPP as a whole. If the unit is set from stop-mode to work-mode, it will continue operations at the exact same point, where it was interrupted before. Currently, pixels, which are already in the pipeline need to be processed by it and cannot be erased. Implementing a global *reset* however, which can be selected in stop-mode, will be part of further evolutions of the design. By default, the EPP is set to stop-mode when initialized after power on.

"1111" - work If the EPP is set to work-mode, it will operate according to its specifications. The process `setOldClk` will run as intended and recognize rising-edges of the incoming PIXELCLK and SYSTEMCLK signals. These rising-edges will furthermore trigger many of the EPP's processes, and new input/output values will be read/written with every PIXELCLK event. The work-mode is temporarily switched back to stop, whenever a signal is transferred via a *Serial Peripheral Interface*¹ (SPI) of the EPP, which will be explained in more detail later on. A failsafe, in order to prevent the EPP from indefinitely remaining in stop-mode, will be implemented in future versions of the design.

"1010" - diag Additional to the work- and stop-modes of the EPP, it also possesses a diag-mode for the diagnosis of the device. If the EPP is set to diag-mode, it will not read input values from its regular energy input ports - which will be connected to the ADC of the WFI - but from an internal diagnosis port (a process called `routeEPPInput` will route the PCU energy input ports to the external EPP or the internal diagnosis port). The internal diagnosis port is provided with energy values coming from the TDGU, which is furthermore connected

¹The SPI protocol is a synchronous serial data link standard and was originally introduced by Motorola. It operates in full-duplex mode, meaning, that it can send and receive data at the same time.

to the CRU. More information about the diag-mode and its functionality will be given in Section 5.3.9, explaining the function of the TDGU.

others / default Each FSM is supposed to contain a default value, which will be realized, if none of the other cases are selected. For the global mode, this default case is the stop-mode. If an erroneous bit-pattern is written into the GMR of the CRU, the EPP will be switched to stop-mode, thus allowing the correction of the control-signal transmission without progressing the pipeline.

Local Workmode

Similarly to the global mode, there is also a local mode, which is valid for each pipeline stage (component) of the EPP. It is implemented as a 32-bit *Local Mode Register* (LMR) in the CRU and distributes groups of four bits to each component of the EPP. Since there are only six units in the EPP design so far, only 24 bit of the available 32 bit are used and more units could be added to the design if necessary. The implementation of the local mode is achieved in several stages. First of all, a process called `setLocalMode` checks the input `LOCALMODE_IN`. A FSM then decides, which mode is realized and stores the corresponding state machine value (work, stop or bypass) in the `LOCALMODE` register. Depending on the value of this register, a second FSM will decide, which tasks the unit is going to perform and what its output will be. Since four bit are available for the coding of the local mode, 13 more modes could be implemented for each component in the current design.

"0000" - stop If a component is in stop-mode, it will not buffer the `PIXELCLK` signal and thus not trigger its processes by a rising-edge. As a consequence, the unit will not perform any operations on the incoming data and merely update its output values to '0'. Also, counting processes will not be triggered and counting signals will remain at the same value. The stop-mode of each single unit could in principle be replaced by the global stop-mode and is mainly a relic from earlier phases of the design, when the global stop-mode was not implemented yet. Updating this configuration is a step, which could easily be conducted in the near future of the device.

"1111" - work If a component is set to work-mode, it will fully operate and conduct all tasks according to its specifications. This is achieved by activating the `setOldClk` process and registration of `PIXELCLK` rising-edges. These signal changes will trigger all functional processes in the respective unit and hence enable full functionality.

"0001" - bypass If a component is set to bypass-mode, the incoming `PIXELCLK` signal is buffered by `setOldClk` and processes are triggered as in work-mode. Each process updating the output though, will distinguish between work-mode and bypass-mode and handle the output accordingly. Whereas for work-mode the incoming signals are manipulated and passed on to other units, in bypass-mode each unit will pass on the raw and unaltered data instead. It is important to note, that data will remain in the corresponding pipeline stage for the same amount of time, no matter whether work-mode or bypass-mode are selected. As a result, the EPP timing does not have to be changed, if one or the other mode is selected, which simplifies

further data handling once the data leaves the EPP. If all pipeline components are set into bypass mode, scientists will be able to look at the raw data stream directly coming from the WFI, which can be an important aid for debugging purposes.

5.2.5 EPP Startup

Due to the pipeline design of the EPP, an incoming pixel will need a certain amount of time to travel through all stages, until it reaches the final output. Consequently, once the EPP is started or initialized, not all components have to work immediately, since the first pixel has not arrived at their respective position in the pipeline. Usually, the time a pixel remains in a certain stage of the pipeline, would be the same for all stages, since each unit has exactly three SYSTEMCLK cycles, until the next pixel arrives. This pattern is realized in each unit of the EPP with the exception of the CMCU. Due to reasons, which will be explained later, the CMCU needs to buffer all incoming pixels of one line, before it can operate properly. As a result, it will not pass on any information to the ETAU, until it has finished its operation for the first time. Once the CMCU has finished its first operation, it will enable a constant input and output data stream. In order to make sure, that a following unit is only operational if the previous unit has passed on valid data, a FSM implemented in the top-level of the EPP, controls their activity after startup. Each unit possesses an input line called VALID_IN, which carries a 1-bit signal and is controlled by a process in the EPP top-level. This process is called `manageStartup` and counts the number of PIXELCLK events, that have been registered by the EPP, in order to "switch on" the units in appropriate time intervals. The number of PIXELCLK events until the PCU is turned on is called `EPP_START_COUNT` and all other signals are chosen in reference to it. Lastly, the `EPP_VALID_OUT` is set to '1' in order to inform the electronics following the EPP, that the first pair of analyzed pixels is ready to be read from its output. Currently, the time, which passes between the startup of the EPP and the first valid pixels at its output, is 140 PIXELCLK cycles. Afterwards, the EPP will supply following electronics with a new pair of pixels for each PIXELCLK event, also across different frames.

5.3 The Components

5.3.1 Top-level

The top-level of the EPP implements all substructures of the pipeline as a structural description in its architecture header. All parts of the pipeline, but the CMCU and the PCU, are instantiated twice, since two pixels are handled at the same time. The CMCU and PCU on the other hand are only instantiated once, but possess two input ports for energy, in order to read two pixels of the same line simultaneously. Aside from defining the components and the general geometry of the EPP, the top-level also defines its entity to the outside. It consists of two 14-bit input ports `EPP_ENERGY_INA` and `EPP_ENERGY_INB`, which will be connected to their respective ADCs of the WFI readout electronics. Since all processes are synchronous to the SYSTEMCLK signal, there are 1-bit inputs `SYSTEMCLK` and `PIXELCLK`, which will be provided by an external sequencer unit, which is also being developed at the IAAT. The respective outputs `EPP_ENERGY_OUTA` and `EPP_ENERGY_OUTB` currently have a width of 64 bit. The 1-bit output `VALID_OUT` was already mentioned in Section 5.2.5 and carries information about the validity of the output signal, which is important for electronics following the EPP. Lastly,

the entity of the EPP contains four SPI protocol related signals, `EPP_SCLK_IN`, `EPP_EN_IN`, `EPP_MOSI_IN` and `EPP_MISO_OUT`. A lot of information like offset values for each pixel of the corresponding WFI sector, as well as threshold values and diagnosis pixel values are stored in the CRU. The 64-bit SPI bus, which was implemented for this version of the EPP, allows the readout and programming of these memories and is controlled by the four aforementioned signal lines. Their exact functionality will be explained in Section 5.3.8.

Aside from the structural description and instantiations of EPP pipeline components, the top-level of the EPP also contains functional elements. There are several processes (like `displayMode` and `displayReceiveSPI`), which implement control functions of the real hardware setup and will be explained in the next chapter. Additionally, the top-level implements processes, which are important for the correct analysis of incoming data. The process `connections` updates the outputs of the EPP with every `SYSTEMCLK` event and maps the corresponding signals of energy, flag-patterns, pixel coordinates and time-stamp to the 64 bits of the output (14-bit energy, 6-bit flag information, 7-bit y-coordinate, 9-bit x-coordinate and 28-bit time-stamp). A process called `setTimestamp` is triggered by the `SYSTEMCLK` signal as well and represents a 28-bit counter. While within its range, it will increase its count by one for every `SYSTEMCLK` event, which is registered. Together with the information about the length of a `SYSTEMCLK` cycle and the number of cycles, that have been completed, it is possible to calculate the time, which has passed since the counter commenced its work.

In future versions of the EPP another input will be added to the entity, allowing to send a reset-signal to the counter. The main time information of the WFI will be calculated by another electronic component, which will reset the time-stamp of the EPP approximately every two seconds, while the time information within these two seconds (and thus 2000 frames), will be calculated by the EPP counter and will be read from the PATSGU for each line of pixels, that completed the EPP analysis.

5.3.2 Pixel Correction Unit

The PCU is the first stage of the EPP pipeline and performs an offset energy correction of each pixel value, which is read from the two inputs `PCU_ENERGY_INA` and `PCU_ENERGY_INB`. It will count the incoming pixels and address an Offset-RAM, which is located in the CRU, via the signal line `PCU_ADDRESS_OUT`. This Offset-RAM consists of two separate block RAMs, each containing a 16-bit offset value for the 32768 pixels of half a WFI sector and can be read from the input ports `PCU_OFFSET_INA` and `PCU_OFFSET_INB`. Bits 0 to 13 contain the energy offset information of each detector element, while bit 15 contains the information if the respective pixel is a *bad pixel* or not. A pixel is called a bad pixel, if it cannot store valid information about its collected charge anymore and is either insensitive to incoming photons or always in *saturation*. Bit 14 does not carry any relevant information and is just due to the 16-bit geometry of each RAM entry.

Offset The offset of a detector describes its intrinsic signal level, which is always present in the different pixels, even if they are not illuminated. It is caused by small variations in either the composition of the pixel's bulk material or the geometry and implementation of the readout nodes and is caused by the fabrication process itself.

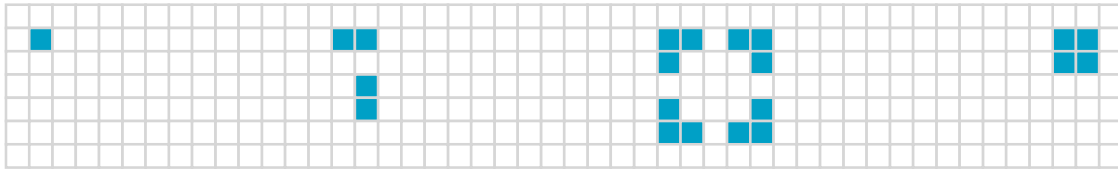


Figure 5.3: Valid pixel patterns for the WFI. The image shows four types of patterns, singles, doubles, triples and quadruples, which will be recognized as valid events by the WFI electronics.

The offset of the detector pixel matrix is calculated by recording so-called *dark frames*, which are frames, that are not illuminated by any photons. Afterwards, the average difference of each pixel to the *baseline value* of the overall pixel array is calculated, thus defining the offset value. The standard deviation of these offset values is called the *noise* of the detector. Consequently, neglecting degradation due to radiation and aging influences, detector offset is constant with time and can be compensated for, by adding (or subtracting) specific offset values to the pixels, while detector noise is a purely statistical effect and cannot be compensated for.

Aside from an offset correction, the PCU also sets a series of flags for each pixel, which are stored in two 3-bit signals and written to the outputs `PCU_FLAGS_OUTA` and `PCU_FLAGS_OUTB`. The corresponding 14-bit threshold values for *Minimally Ionizing Particles* (MIP) and *misfits* are read via passive signal lines `PCU_MIP_IN` and `PCU_MISFIT_IN` from registers in the CRU. If the respective threshold values are exceeded by the energy value of the pixels, the corresponding flag is set to '1', or remains '0' otherwise. The sequence of flags from lowest to highest bit is bad pixel flag, misfit flag and MIP flag.

MIPs MIP events are caused by ionizing particles from surrounding radioactive sources or cosmic radiation and will deposit energy in the pixels of a photon detector. Usually they have very high speeds and cannot be completely stopped by a single pixel. As a consequence, they will travel through the detector material, depositing part of their energy in each pixel they cross, before leaving the detector again. MIP events can therefore be distinguished from real photon events, since they will leave a trail of almost constant energy in each pixel they pass and are therefore recognized as invalid patterns on the detector (refer to Figure 5.3).

Misfits Misfit events can occur if a photon hits a pixel during its readout process. Typical readout schemes will sample the pixel's signal multiple times, before clearing it and sampling the baseline for the same amount of times. If a photon hits the pixel during or before baseline sampling, the baseline will be lifted up to higher energies, which can even exceed the energy deposited by another photon prior to the readout. As a consequence, when the baseline is subtracted from the pixel energy, the resulting value will be negative. The ADC will recognize this constellation and assign a predefined, very low energy value to the pixel, which can be

discriminated by the EPP's misfit threshold value later-on.

The subtraction of the offset value and the setting of the flag signal for each pixel is conducted by the main working process `correctPixel`. Before the offset value is subtracted, a constant value of 16384 ADU is added to the energy value of the pixel in order to assure, that no negative values are caused by the correction and to keep the relative energy difference between all pixels constant. The 14-bit signal is thus increased to 15 bit of information.

The inputs `PCU_WINDOWSTART_IN` and `PCU_WINDOWWIDTH_IN` are connected to registers in the CRU and will be fully implemented in later stages of the EPP. The final version of the EPP is foreseen to have a functionality called *window-mode readout*, which will not read out the whole WFI sector, but only a small area. The value of `PCU_WINDOWSTART_IN` will define where the corresponding window will start (line numbers from 0 - 511) and `PCU_WINDOWWIDTH_IN` will represent the number of lines the window will consist of.

5.3.3 Common-Mode Correction Unit

The CMCU differs from all other pipeline stages of the EPP in many aspects and marks the second unit a pixel passes during its analysis. Just like the PCU, it is only instantiated once and contains two energy inputs, `CMCU_ENERGY_INA` and `CMCU_ENERGY_INB`. Furthermore, it receives the flag information of the PCU via the signal lines `CMCU_FLAGS_INA` and `CMCU_FLAGS_INB`. The design of the CMCU, as well as the hardware implementation of the algorithm it uses for sorting, represents one of the biggest challenges of this thesis, but has also led to a new concept of high-speed common-mode correction for pixelated photon detectors.

Common-mode As already described in Chapter 2, the DEPFET pixel array of the WFI will be read out one line at a time. During this readout, every pixel of the line is furthermore amplified with the same gain factor, which is dependent on the electronic's supply voltage. This supply voltage however, will be exposed to small fluctuations, variable with time. Consequently, different lines, which will be read out at different times, will be amplified with slightly different gain factors, a phenomenon, which is called the *common-mode*. The resulting energy difference in each line, in reference to other lines, is the same for each pixel and called the common-mode offset.

One way to effectively correct for common-mode offset, is to subtract the median value of a set of detector pixels from each pixel within the set. Before the subtraction however, the CMCU will increase the pixel energy value by 32768 ADU and therefore the dynamic range of the energy. The median value itself is the numeric value, which separates the higher half (referring to the value) from the lower half of a set of numbers. One very effective way of finding the median is to sort these numbers and look at the innermost element(s) of the sorted set. Unfortunately, pixels entering the EPP are not yet sorted by their energy value, but only by their position in the WFI sector. Also, sorting a set of numbers is only possible, if the set is complete and no new numbers will be added later-on. Consequently, in order to sort the energy values of a line of a WFI sector, it is necessary to wait, until all pixels of the line have arrived in the CMCU and store all previous pixels in the meantime. Furthermore, while the CMCU manipulates stored pixels of one line, new pixels will be entering the CMCU, which

also need to be stored and manipulated later-on. The functionality of the CMCU is highly time-critical, since there will only be limited amount of memory to buffer incoming lines, which have not been processed yet. The fact, that each of these lines consists of 128 14-bit values plus 3 bits of flags for each pixel, will cause the utilization of many Configurable Logic Blocks (CLBs), if the information is stored in registers or distributed RAM. Aside from the memory usage problem, there is the problem of the available time for sorting the 128 pixel energy values. Even the fastest sorting algorithms like *quick-sort*, cannot sort faster than $N = n \cdot \log(n)$, where n is the number of elements, that need to be sorted and N is the number of processing steps needed to fully sort the set. In case of the 128 pixels this leads to an amount of

$$N = 128 \cdot \log(128) = 269.72 \quad (5.2)$$

clocks. Due to the fact, that the CMCU is getting two pixels at a time, there are only 64 PIXELCLKs available for the whole operation, which translates to 196 SYSTEMCLKs and shows, that even processes, which are triggered by the SYSTEMCLK signal cannot perform enough operations to completely sort the set of energy values in time. A solution to this problem, lies in the parallel processing capabilities of the FPGA. Since it is possible to instantiate multiple comparators at the same time, 64 pairs of numbers can be sorted simultaneously. An algorithm implementing this idea and enabling the usage of parallel architectures is the so-called *Odd-Even Transposition Sort* (OETS) (Thomson Leighton, 1991). In the framework of this thesis, the OETS has been implemented in hardware for the first time at the IAAT.

Odd-Even Transposition Sort Algorithm

The idea of the OETS is to reduce the sorting of a whole set of numbers, to the comparison of alternating pairs of neighboring numbers. For a set of n numbers in n slots, n being an even natural number, $n/2$ pairs are created. In a first step, the *odd step*, slots 0 and $n - 1$ are paired, as well as slots 1 and 2, 3 and 4, ..., and $n - 3$ and $n - 2$. For each of these pairs the algorithm switches the position of the smaller number to the left and the larger number to the right. For equal numbers, nothing will happen. In sequential processing this process would be very slow, since only two numbers are sorted at a time and a lot of pairs need to be handled separately. With the parallel processing abilities of an FPGA however, all these pairs can be compared within the same clock cycle, thus sorting $n/2$ pairs of numbers in one clock.

In the next step of the algorithm, the *even step*, pairs are changed and slots 0 and 1, 2 and 3, ..., and $n - 2$ and $n - 1$ are sorted. Again, the FPGA can conduct this step with just one single clock and sort all pairs simultaneously. The two steps are now repeated multiple times, until the whole set of numbers is sorted. In a worst case scenario, this algorithm will sort a set of n numbers in n time-steps, if implemented on an architecture with $n/2$ processing units. Thomson Leighton (1991) show, that the OETS will eventually sort any linear array of n numbers in n steps and therefore only grows linearly with the number of sorting elements for a parallel architecture (refer to Figure 5.4 for an example).

Considering the linearity of the OETS, it is possible to sort the 128 pixel energy values of one WFI sector line in 128 clocks. If the sorting process is triggered by the SYSTEMCLK signal, 196 clock cycles will available for operation, thus enabling the sorting of the whole array in

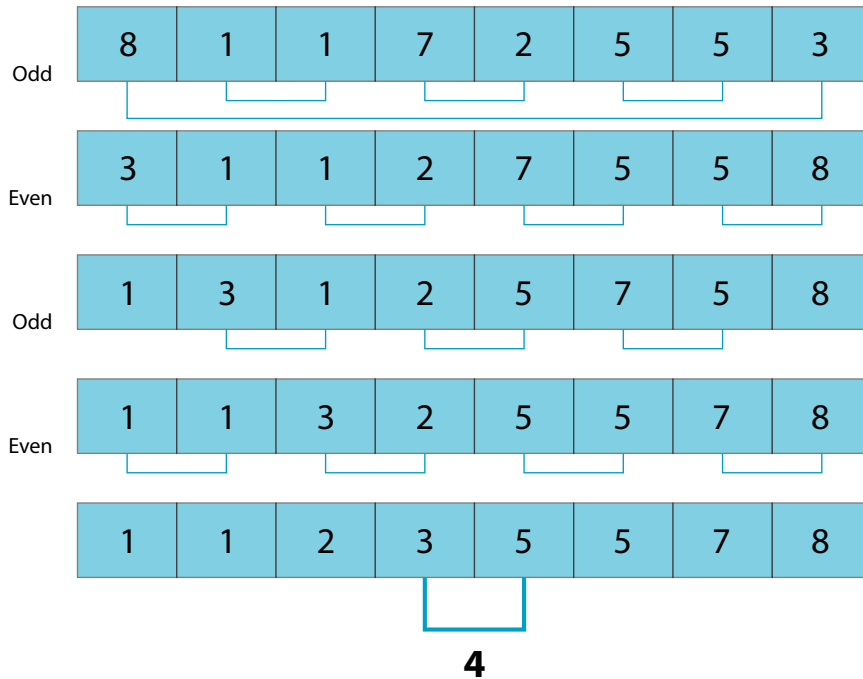


Figure 5.4: Example of the OETS algorithm for a parallel processing architecture, with multiple comparison threads. Here, eight arbitrary numbers are sorted in four clock cycles and a median of 4 is calculated.

less time than is available. Consequently, the time issue of the CMCU is solved, and an array of 128 values can be sorted, while the next line is being read from the input ports. In VHDL, the OETS algorithm is implemented by the utilization of a *loop statement*, which will cause the instantiation of multiple comparator units for each pair of numbers (refer to code extract in Figure 5.5).

Aside from the timing problem, there is also the problem of memory usage and occupation of CLBs, which will slow down the overall performance of the EPP. One problem, that arises in this context is, that pixels are continuously entering the pipeline and that a completed line, needs to be copied and sorted immediately, since its memory will be overwritten by new incoming data otherwise. Additionally, once the line is sorted, it has to be written to the output of the CMCU, pixel by pixel, but in its initial unsorted order, since this order represents the way pixels were arranged on the detector and is needed for image reconstruction later-on. As a result, for continuous operation of the CMCU, four memories are needed, in order to store all pixel information during input, sorting and output.

In the initial design phases of the CMCU, incoming pixels were stored in a 128 x 19-bit register and then copied to two further registers, one for sorting and one for the conservation of the initial order. The median was calculated from the sort-register and subtracted from the initially ordered pixel values. Lastly, the median-corrected register was copied to a fourth register and written to the output, pixel by pixel. As a result, the CMCU design itself already used up 9728 flip-flops, which attributed to a usage of approximately 65% of slices of the FPGA. Since the design was just in its initial stages at that time, a utilization of that many resources had to be avoided in order to leave room for further implementations and a more

Odd sort

```

for i in 1 to 63 loop
  if MEDIAN_REGB((2*i)-1) > MEDIAN_REGB(2*i) then
    MEDIAN_REGB(2*i)          <= MEDIAN_REGB((2*i)-1);
    MEDIAN_REGB ((2*i)-1)    <= MEDIAN_REGB (2*i) ;
  end if;
end loop;

```

Even sort

```

for i in 0 to 63 loop
  if MEDIAN_REGB(2*i) > MEDIAN_REGB((2*i)+1) then
    MEDIAN_REGB(2*i)          <= MEDIAN_REGB((2*i)+1);
    MEDIAN_REGB ((2*i)+1)    <= MEDIAN_REGB (2*i) ;
  end if;
end loop;

```

Figure 5.5: Extract from the CMCU source code. This part of the source code represents the implementation of the two sorting states of the OETS algorithm. It is clearly shown, that both sorting stages only differ in terms of the chosen number pairs, but are identical otherwise.

efficient RAM arrangement and control structure had to be invented. Block RAMs do not use up CLBs, since they represent additional structures in the FPGA, but are much slower than registers. Furthermore, RAMs cannot be copied in just one clock cycle, but would have to be addressed and read entry by entry. Also sorting many paired values at once would not be possible with block RAM. Instead, in order to save resources of the FPGA, some of the old registers, where performance was not an issue, were replaced by block RAM in order to save FPGA resources.

5.3.4 RAM Control and Memory Management of the CMCU

The final design of the memory structure in the CMCU uses six dual-ported block RAMs of 64 x 19 bits, which are grouped into three units MEDIAN_RAMAO, MEDIAN_RAMAI and MEDIAN_RAMAI2. Furthermore, two 128 x 16-bit registers, MEDIAN_REGA and MEDIAN_REGB are implemented for fast operation, as well as three 16-bit registers, MEDIANA0, MEDIANA1 and MEDIANA2 for the storage of calculated median values. The total amount of bits provided by logic cells is limited to the contribution of the registers and adds up to 4864 flip-flops, which is only half of the amount of the initial design. The operation is controlled by a FSM, which controls a state called RAMSTATE with possible values rama0, rama1 and rama2 and also switches the *Write-Enable* signals (WEA and WEB) for each RAM. Since block RAMs cannot write two pixel values at the same time, the solution was to group two single RAMs (like MEDIAN_RAMAO0 and MEDIAN_RAMAO1 for example), so that two ports could be addressed and written simultaneously. In the current design, CMCU_ENERGY_INA and CMCU_FLAGS_INA are connected

to the first RAM of each group (MEDIAN_RAM_A00 and MEDIAN_RAM_A10 and MEDIAN_RAM_A20), while CMCU_ENERGY_INB and CMCU_FLAGS_INB are connected to the second (MEDIAN_RAM_A01 and MEDIAN_RAM_A11 and MEDIAN_RAM_A21). Also, CMCU_ENERGY_INA and CMCU_ENERGY_INB are connected to cells 0 - 63 and 64 - 127 of MEDIAN_REGA.

After startup, the CMCU will have a RAMSTATE of `rama0` (controlled by a process called `changeRamState`, which uses the counted amount of pixels by `countPixels`) and incoming data (referred to as pixelset 1 in this example) will be written into the RAM group MEDIAN_RAM_A0 and MEDIAN_REGA simultaneously by a process called `sortIntoRegARamA`. While all incoming data is written into the block RAM, only the energy values of each pixel are copied into the register, in order to save CLBs. Once the line is completed, MEDIAN_REGA will be copied into MEDIAN_REGB and RAMSTATE will be switched to `rama1`. Now, the newly incoming pixelset 2 will be copied to RAM group MEDIAN_RAM_A1 and MEDIAN_REGA, while a process called `sortPixelValues` will start sorting the pixel values in MEDIAN_REGB. Once the sorting process is finished (after 128 SYSCLK cycles), the resulting median value will be copied into the register MEDIAN_A0, which denotes, that this median value corresponds to the set of pixels stored in MEDIAN_RAM_A0. When the input of pixelset 2 is finished, MEDIAN_REGA is again copied to MEDIAN_REGB and RAMSTATE is switched to `rama2`. Now, incoming pixelset 3 is copied into MEDIAN_RAM_A2 and MEDIAN_REGA, while pixelset 2 in MEDIAN_REGB is sorted. At the same time, pixelset 1, whose median has been calculated and whose original values were stored in MEDIAN_RAM_A0, is written to the outputs of the CMCU. When the input of pixelset 3 is finished, all pixels from MEDIAN_RAM_A0 have been passed on to the ETAU, making this RAM available for further input. Consequently, the RAMSTATE will switch back to `rama0` and the incoming pixelset 4 will be written to MEDIAN_RAM_A0, while pixelset 3 is sorted and pixelset 2 is written to the output. This interaction of RAMs and registers will continue in the same pattern, until all pixels of all frames are processed. It is furthermore illustrated in Figure 5.6.

5.3.5 Energy Threshold Analyzer Unit

The ETAU is implemented as the third pipeline stage and will get 16-bit energy values from the CMCU via the ETAU_ENERGY_IN input. Instead of having two input ports, it is instantiated twice, which provided a better clock frequency performance for the synthesis of the design. Additionally, it has an input ETAU_FLAGS_IN for the 3-bit flag values of each pixel, as well as two passive signal lines, ETAU_CRU_LOWER_IN and ETAU_CRU_NEIGHBOR_IN providing 16-bit *low energy threshold* and *neighbor threshold* values from the CRU. The main working process `analyzeThresholds` is implemented as a FSM, which remains in an idle state until a PIXELCLK event is recognized and the current input signals are buffered for further processing. At the same time, the already processed values are written to the output ETAU_ENERGY_OUT. Afterwards, it changes into a state, where the buffered energy value of each pixel is compared to the respective threshold values and flags are set accordingly. These flags are added to the already existing flags from the PCU, increasing the 3-bit signal to five bits. In order to account for this change in signal width, the respective output for flags of the ETAU is called ETAU_FLAGPATTERN_OUT instead of ETAU_FLAGS_OUT.

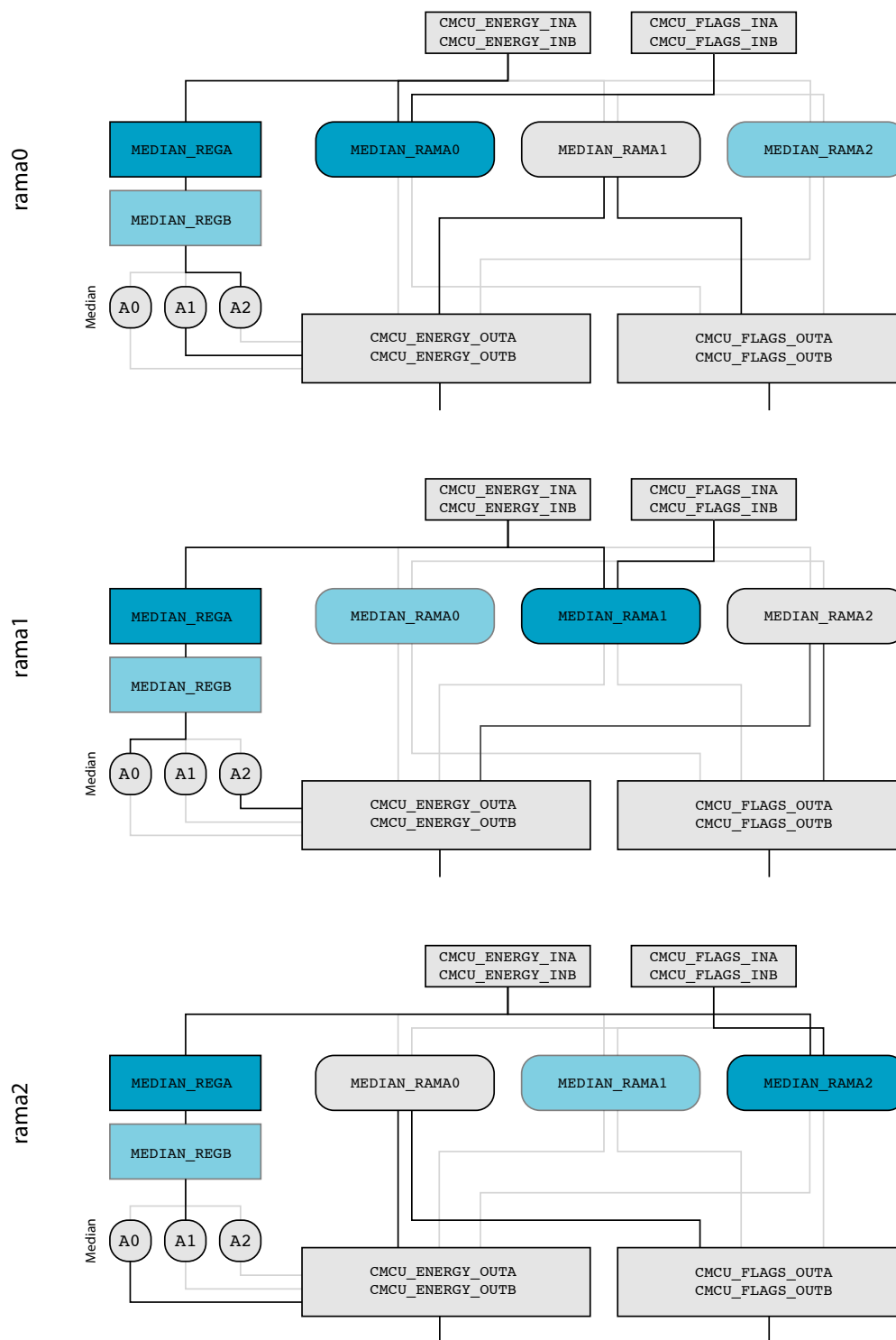


Figure 5.6: Illustration of the CMCU RAM and register control for all three RAMSTATES, rama0, rama1 and rama2. Gray signal lines are inactive for the respective RAMSTATE, while black signal lines denote active lines. Alike colors denote, that these components contain values of the same line of pixels.

Lower Energy Threshold The value for the lower energy threshold describes the amount of signal charge, which is needed, in order to recognize the information of a pixel as a real event. In Chapter 2 it was already mentioned, that incident photons will cause electron-hole pairs in the bulk material of the detector. For X-rays, the amount of electron-hole pairs is in the range of hundreds or thousands, while typical values for thermally induced electron-hole pairs are on the order of tens of pairs. As a result, noise and valid signals can be distinguished by setting a minimum energy, which needs to be deposited in a pixel, in order to render it as a valid event. If a pixel's energy exceeds the lower threshold, its according flag will be set to '1'.

Neighbor Threshold The neighbor threshold is introduced due to the circumstance, that electron-hole pairs do not have to be confined underneath one single pixel, but can also spread across multiple pixels in a total of four valid patterns, even if just one pixel was hit. If the resulting charge cloud gathers underneath two neighboring pixels for example, the event is called a double event and the energy of both pixels needs to be summed up in order to find out about the energy of the incident photon. The ratio in which the energy is split between the two pixels is not constant and can vary greatly. As a result, since each pixel is analyzed individually by the EPP, pixels, which only got a small fraction of the energy in a multi-pixel event, would be discarded as not meeting the lower threshold. If this happened, it would not be possible to reconstruct the real energy of the event from the pixel pattern, making it necessary to implement another threshold value, the neighbor threshold, which is lower than the lower energy threshold². If a pixel is flagged as meeting the neighbor threshold, but not the lower threshold, it will be investigated in further stages of the readout electronics of the WFI, where more elaborate pattern analyses are conducted.

After being processed by the ETAU, the updated flag-pattern sequence for each pixel will be bad pixel flag, misfit flag, MIP flag, neighbor flag and lower threshold flag from lowest to highest bit.

5.3.6 Programmable Pixel Filter Unit

The PPFU marks the fourth stage in the EPP pipeline and performs an analysis of each pixel's flag-pattern, which is passed on from the ETAU via the PPFU_FLAGPATTERN_IN signal line. It is instantiated twice and also gets the 16-bit pixel energy via its PPFU_ENERGY_IN input, but does not manipulate this value. Instead it compares the incoming flag-pattern of each pixel, with a reference pattern, called the *filter-mask*, which is read from the passive signal input PPFU_FILTERMASK_IN and is stored in a register of the CRU. The main process `filterPixel` is implemented as a FSM, which remains in an idle state, until it is triggered by a rising-edge event of PIXELCLK. Once the process is triggered, it will buffer all incident input signals and simultaneously update the unit's outputs PPFU_ENERGY_OUT and PPFU_FLAGPATTERN_OUT with already analyzed values from the previous PIXELCLK cycle. It is important to note,

²Specific energy values for the respective thresholds will be finalized in the calibration phase of the IXO mission and are currently only implemented as dummy values.

that the bit-width of `PPFU_FLAGPATTERN_OUT` is increased by one bit in reference to `PPFU_FLAGPATTERN_IN`, which is due to the fact, that the PPFU will add another flag to the already existing flag-pattern, the so-called *valid flag*. If the incoming flag-pattern from the ETAU matches the user-defined filter-mask, the pixel will be marked as valid or invalid otherwise. The valid flag is the most important information, next to the energy of the pixel, since it will ultimately decide, if the corresponding pixel information will be transmitted to the ground stations or not.

5.3.7 Pixel Address and Time-Stamp Generator Unit

The PATSGU marks the last stage in the EPP pipeline and prepares the incoming pixel data for ground transfer. For this purpose, it receives the information about pixel energy via `PATSGU_ENERGY_IN`, pixel flag-pattern via `PATSGU_FLAGPATTERN_IN`, the starting-row for window-mode readout via `PATSGU_WINDOWSTART_IN` and the current global EPP time-stamp via `PATSGU_TIMESTAMP_IN`. A process called `countPixelsCreateLineCLK` counts all incoming pixels. Whenever it reaches pixel 0 of a particular line, the time-stamp, which is generated by the top-level of the EPP, is read from the unit's input and buffered for further operations. The main process `generateEventPackage` is implemented as a FSM, which is in idle mode until a `PIXELCLK` event occurs. Equal to the ETAU and PPFU it will buffer all incident signals, while updating the outputs `PATSGU_ENERGY_OUT`, `PATSGU_FLAGPATTERN_OUT`, `PATSGU_X_OUT`, `PATSGU_Y_OUT` and `PATSGU_TIMESTAMP_OUT` with the already processed values. It will furthermore calculate a pixel address for each pixel, which is handled. Since all pixels will be passing the unit sequentially, their corresponding position on the detector is related to their position in the pipeline. With the information of `PATSGU_WINDOWSTART_IN`, the unit "knows" the address of the first pixel entering the unit. Each line has 128 (0 - 127) pixels, so line n will start with pixel number $(n - 1) \cdot 127$. By adding the information of x and y-coordinates to each pixel, it is possible to identify any pixel's position in the sector and later-on reconstruct the corresponding photon image.

5.3.8 Control and RAM Unit

The CRU can be described as the "brain" of the EPP, since it contains all RAMs and registers, storing important information for its operation. It did not belong to the original *D3C EPP* design for Symbol-X, but was implemented as a part of this thesis. The CRU is connected to the PCU, ETAU, PPFU and TDGU and exchanges data via multiple signal lines. It contains two offset value LUTs for the PCU, `offsetRamA` and `offsetRamB`, each with 32768 cells of 16-bit depth, two testmask LUTs for the TDGU, each with 32768 cells and 1-bit depth, as well as a total of twelve 32-bit count registers and eight 16-bit threshold, filter-mask and setup registers. Initially, each unit of the EPP was foreseen to have its own RAM and registers, which could be programmed via SPI, but due to reasons of performance and structure, it was decided to move all EPP memory into one single unit. As a result, the EPP only needs to implement SPI communication for one unit, thus only requiring one *address decoder* and furthermore saving CLBs. The signals `EPP_SCLK_IN`, `EPP_EN_IN`, `EPP_MOSI_IN` and `EPP_MISO_OUT` are directly connected to the CRU's `SPI_SCLK_IN`, `SPI_EN_IN`, `SPI_MOSI_IN` and `SPI_MISO_OUT` ports. SPI communication between external sources and the EPP's CRU can be established by setting the `EPP_EN_IN` input to 'low', since it is 'high' by default.

A process in the CRU called `writeCRUOut`, which updates the passive signal lines of the CRU to other units with every `SYSTEMCLK`, will switch the EPP into stop-mode, so that received SPI information will not interfere with ongoing EPP operations. In order to make sure, that a damaged `EPP_EN_IN` signal line will not indefinitely set the `GLOBALMODE` into stop-mode, a *failsafe mechanism* will have to be implemented in future versions of the design. One possible solution could be to select stop-mode only, if the transmitted SPI command is valid. Afterwards, the SPI will be ready for data reception and will record single bits from its input `EPP_MISO_IN` with every clock cycle from `EPP_SCLK_IN`. A complete SPI signal of the EPP consists of 64 bits and is interpreted by the process called `spi`. It is implemented as a FSM and starts in a state called `readIOSignal`, which interprets the first four bits as the *input mode* of the transmission and can have values for output (0000) and input (0001). Since these four bits are read in different clock cycles, a counting variable `IOSIG_BITCOUNTER` will count the amount of bits already transmitted and store them in a buffer called `IOSIG_BUFFER`. After reading the I/O signal, the FSM will switch to a state called `readAddress`, which will interpret the next 28 bits as an address (counted by `ADDRESS_BITCOUNTER`). Each register and RAM cell has their own address, which will be decoded by an address decoder, and thus selected for input or output. Once the address is read, the FSM will switch to a state called `readData`. It will count the next 32 incoming bits (`DATA_BITCOUNTER`) and store them in a buffer called `DATA_BUFFER`. Now that the SPI transfer is complete, the process will switch to a state called `executeSPI`, which represents the address decoder. It will analyze the 28-bit address information and select the corresponding memories (an illustration of a complete SPI command transmission is given in Figure 5.7).

In order to increase readability, the 28-bit information is expressed in hexadecimal notation. Memories and registers are furthermore grouped by the highest three hex values (group bits), meaning, that the lowest four hex values can select several memories within a group. A complete list of all registers and RAMs in the CRU is given in Table 5.1, as well as their corresponding address and bit-width. It can be seen, that some of these registers only store 16-bit information, even though the data, which is transferred by the SPI contains 32 bits. This is due to the very simple structure of SPI, which is easy to implement on almost any hardware, but is not very flexible in terms of reading or writing non-uniform data. As a result, a lot of times unnecessary data is transmitted and in order to read from an internal register, the SPI communication has to be executed twice, once with a dummy signal, until data arrives at the `EPP_MISO_OUT` port. Since the SPI was only implemented for testing purposes and will not exist in the final design of the EPP, this circumstance does not contradict the high-speed data transfer rates and limitation of bandwidth of the WFI. Instead a more refined and adapted protocol will be used for the communication with the EPP's registers and RAMs in the final design.

The address selection itself is implemented in a case structure, which investigates the group bits of each transferred address. After the group is selected, another case structure analyzes the lowest four hex values and decides, which memory will be selected. Once the selection is complete, the I/O signal is checked. If the SPI command is an input command, it will copy the contents of `DATA_BUFFER` into the corresponding register or RAM. In case of RAMs, also the write-enable signals are set accordingly, so that cells in the RAM can be written. If output is selected, the contents of the selected register will be copied into another 32-bit register, called `DATAOUT_REGISTER`. This register however, will not be written to the output

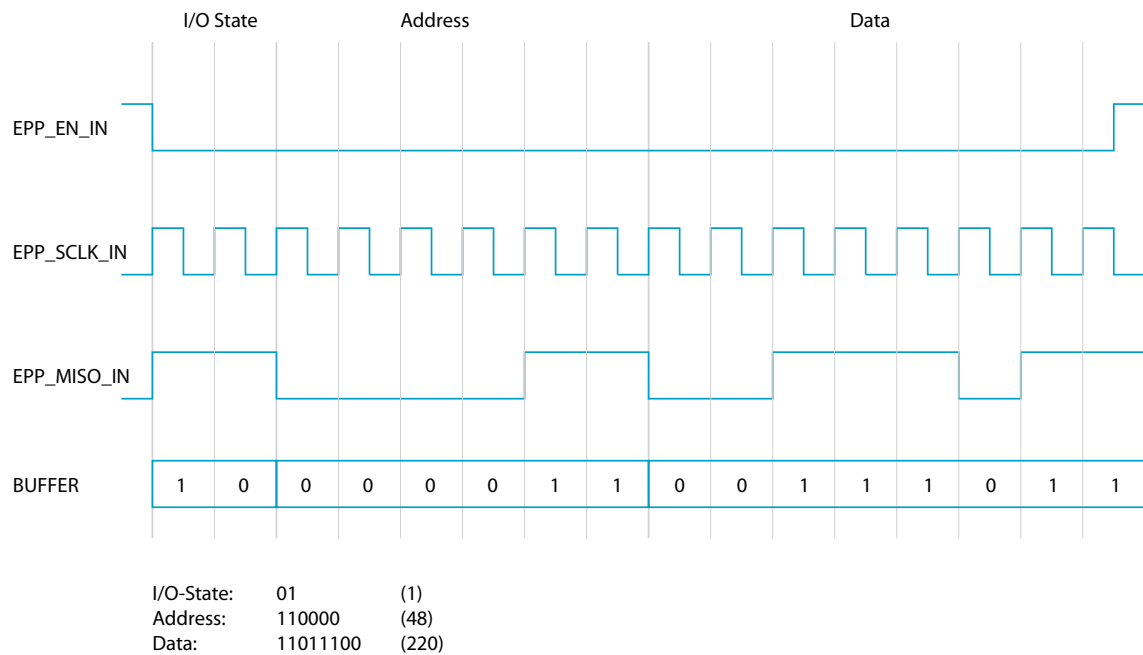


Figure 5.7: Illustration of an SPI command transfer with a 16-bit SPI. The first two bits are used as an I/O signal, the next six as an address and the last eight bits are used as data. It can also be seen, that the first transferred bit is the lowest bit of the corresponding value.

EPP_MISO_OUT immediately, but bit by bit with every SCLK event, while the new command is being read. Consequently, if just one value has to be read from the CRU, two SPI commands have to be transmitted, one containing the output mode and the address of the register, as well as dummy data and one 64-bit dummy signal. In order to prevent misinterpretations of an SPI signal in case not all 64 bits are transferred correctly, the states `readIOSignal`, `readAddress` and `readData` will return to the `idle` state, in case `EPP_EN_IN` is set to 'high' during their respective execution.

All RAMs, which are implemented in the CRU, are *dual-ported RAMs* and can be read and written at the same time on two separate ports A and B (as long as not the same cell is read and written at once, a situation which is called a collision). The advantage for the EPP is, that two different cells of each RAM can be used internally (by the CRU and SPI) as well as externally (by the units, which utilize the RAM's information) with dedicated wiring. External connections for readout are always connected to the B-port of each RAM, with the write-enable signal always turned off. Also the data-in signal lines for each RAM are set to a constant value of zero. The A-port of each RAM on the other side, is wired to the internal connections of the CRU and is used for data input via SPI. Its write-enable status is set by the `spi` process as explained above.

Another task of the CRU is to count pixels, which have been flagged as bad pixels, misfits, MIPs, beneath the lower threshold or exceeding the neighbor threshold and - if matching the filter-mask in the CRU - as valid. For this purpose, the CRU contains "hard-wired" signal lines from both instances of the PPFU to the CRU. A process called `countPixelsFromCRU`,

Table 5.1: A list of all memories in the CRU with their respective address ranges, bit-width and unit connections.

Name	Connection	Width	Address
offsetRamA	PCU	16 bit	x000 0000 - x000 1FFF
offsetRamB	PCU	16 bit	x001 0000 - x001 1FFF
WINDOWSTART_REGISTER	PCU, PATSGU	16 bit	x004 0000
WINDOWWIDTH_REGISTER	PCU, PATSGU	16 bit	x004 0001
MIP_REGISTER	PCU	16 bit	x005 0000
MISFIT_REGISTER	PCU	16 bit	x005 0001
NEIGHBOR_REGISTER	ETAU	16 bit	x005 0002
LOWER_REGISTER	ETAU	16 bit	x005 0003
FILTERMASK_REGISTER	PPFU	16 bit	x006 0000
PPFU_COUNT_BADPIXELSA	PPFU	32 bit	x006 0001
PPFU_COUNT_MIPSA	PPFU	32 bit	x006 0002
PPFU_COUNT_MISFITA	PPFU	32 bit	x006 0003
PPFU_COUNT_LOWERTHRESHA	PPFU	32 bit	x006 0004
PPFU_COUNT_NEIGHBORTHRESHA	PPFU	32 bit	x006 0005
PPFU_COUNT_VALIDSA	PPFU	32 bit	x006 0006
PPFU_COUNT_BADPIXELSB	PPFU	32 bit	x006 0007
PPFU_COUNT_MIPSB	PPFU	32 bit	x006 0008
PPFU_COUNT_MISFITB	PPFU	32 bit	x006 0009
PPFU_COUNT_LOWERTHRESHB	PPFU	32 bit	x006 000A
PPFU_COUNT_NEIGHBORTHRESHB	PPFU	32 bit	x006 000B
PPFU_COUNT_VALIDSB	PPFU	32 bit	x006 000C
testmaskRamA	TDGU	1 bit	x007 0000 - x007 1FFF
testmaskRamB	TDGU	1 bit	x008 0000 - x008 1FFF
TDGU_SETUP_REGISTER	TDGU	16 bit	x009 0000
GLOBALMODE_REGISTER	top-level	4 bit	xFFF 0000
LOCALMODE_REGISTER	all units	32 bit	xFFF 0001



Figure 5.8: Standard 1-bit, 512 x 128 pixels test-mask of the TDGU RAM. Black marks areas where pixels are hit, while white areas mark pixels, that will be mapped with noise energy values.

which is triggered by `PIXELCLK` events, analyzes the transferred flag-pattern for each pixel and will increase the counters accordingly. The information stored in these counters, which can be used as a checksum or just for additional statistical purposes, can be read out via SPI after a sequence of frames has been analyzed.

5.3.9 Test Data Generator Unit

The TDGU was implemented as a diagnosis tool for the EPP and enables the testing of EPP units even without external pixel data input. In an initial design, the TDGU was intended to contain a fixed RAM of 512 x 128 pixel values, but due to the connected utilization of large portions of block RAM, another idea was pursued. Instead of 512 x 128 14-bit energy values, the TDGU accesses a RAM in the CRU, which contains 512 x 128 1-bit values (RAM is again split into two separate block RAMs to enable the transmission of two pixel values simultaneously), serving as a mask and marking pixels, that have been hit by a "test-photon". Energy values and noise values are furthermore stored in the TDGU itself and can be mapped onto the corresponding pixels of the mask, depending on a setup (which is read from the input `TDGU_SETUP_IN`), which is chosen for the diagnosis. Currently, three different setups have been implemented in the TDGU with four distinct energy values for hit pixels `DIAG_ENERGY_0`, `DIAG_ENERGY_1`, `DIAG_ENERGY_2` and `DIAG_ENERGY_3`, as well as four different noise values `DIAG_NOISE_0`, `DIAG_NOISE_1`, `DIAG_NOISE_2` and `DIAG_NOISE_3`. On startup, a standard test-mask is loaded into `testmaskRamA` and `testmaskRamB` of the CRU (see Figure 5.8), which can be changed via the SPI of the CRU. The mask values are addressed via the address signal line `TDGU_ADDRESS_OUT`, which addresses both RAMs for upper and lower part of the WFI sector simultaneously. The corresponding mask values are transferred via the input ports `TDGU_TESTMASK_INA` and `TDGU_TESTMASK_INB`. With every `PIXELCLK` event, the TDGU writes either the information for a hit pixel or noise to the outputs `TDGU_ENERGY_OUTA` and `TDGU_ENERGY_OUTB` of the unit, where they can be read by the PCU. The decision whether pixel values are read from the external inputs of the EPP or the internal ports of the TDGU is dependent on the `GLOBALMODE` and controlled by a top-level process called `routeEPPInput`.

6 Simulations, Hardware Synthesis and First Results

In the framework of this thesis, all steps, which were described in Chapter 4 have been completed in order to produce a first working prototype of the EPP. Even though not all final functionalities are implemented in the current design yet, the prototype can serve as a proof of concept and, with further critical performance testing in combination with a real detector, even as a performance verification model. More information about this will be given in Chapter 7.

Since Chapter 5 focussed on the design aspect of the EPP, this chapter will now focus on the hardware implementation, the conducted software and hardware testing, as well as the first results of these tests.

6.1 Software Testing

In hardware design it is common to perform elaborate software-based testing before switching to hardware implementation. In case of the EPP prototype, software testing was performed with the help of test-benches (refer to Figure 6.1 for an example), which were already described in Paragraph "**Description via HDLs**" of Section 4.4. One disadvantage of using a test-bench as a testing platform for hardware is, that incoming data has to be manually generated. In case of the EPP, one frame of a detector stripe consists of 32768 pixels with 14 bit each and every 30 ns, two new pixels have to be available at the inputs. Consequently, thorough testing of the EPP's functionality can only be achieved when using predefined data-sets. For this thesis, data-sets were compiled with small, dedicated C-programs, which generated alternating pixel patterns with pixel values ranging from zero to the dynamical range limit and wrote them into text-files. Two such files were created simultaneously, one for the A and B input ports of the respective unit each. For units, which are instantiated twice in the pipeline (ETAU, PPFU, PATSGU), just single tests with single input files were performed, since the second instantiation does not differ from the first one and does not offer any new insights in its functionality. In total, seven test-benches for the PCU, CMCU, ETAU, PPFU, PATSGU, CRU and the EPP top-level have been implemented so far, with over 1600 lines of source code. Each test-bench contains two processes, called `read_input` and `write_output`, which handle file input and output. Another process, which exists in all units is the `startUnit`-process, which sets their `VALID_IN` port to 'high' and therefore tells the unit, that the next incoming pixel will be a real pixel value coming from the ADC. Simultaneously with the setting of this signal, the first pixel or set of pixels is read from the input text-file. Lastly, all test-benches define `PIXELCLK` and `SYSTEMCLK` periods as 30 ns and 10 ns respectively. Processes, which switch the respective clock signal from 'high' to 'low' every half-period are called `SYSTEMCLK_process` and `PIXELCLK_process`, despite the EPP top-level, where this

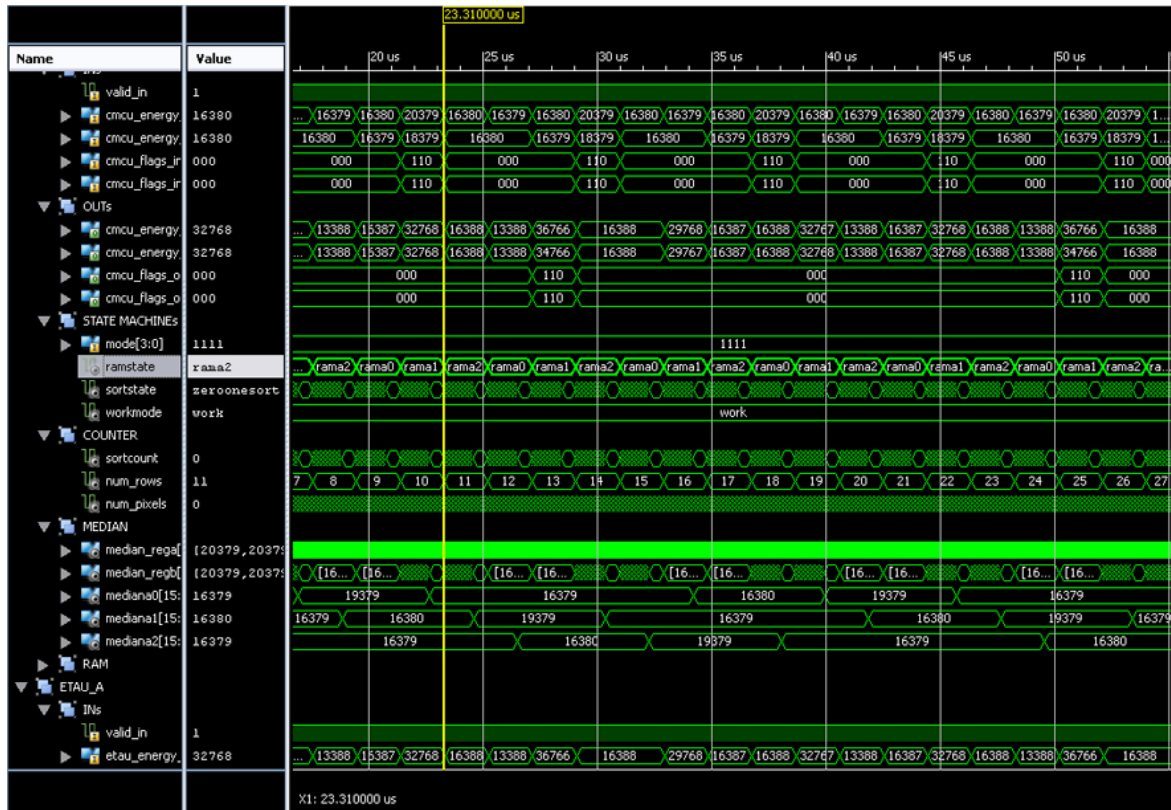


Figure 6.1: Exert from the CMCU test-bench simulation. The screenshot was taken with the Xilinx ISim VHDL simulation software. On the left hand side of the image, all signal names as well as their current values (yellow line marks the current time in the simulation) can be seen. The right hand side shows the time development of each signal, as well as the contents of registers and how they change. In this exert, a lot of RAMSTATE cycles are passed, which can also be seen from the NUM_ROWS signal, which counts the lines that have entered the CMCU. Simulations like this are used for every test-bench, in order to find out, if the corresponding units behave correctly.

process is called `CLK_process`, due to the utilization of a *Digital Clock Manager* (DCM), which generates a synchronous `SYSTEMCLK` and `PIXELCLK` out of the top-level `CLK` signal.

In order to enable the quick investigation of the input and output files of the test-benches, another heritage from the EPP of Simbol-X was used. With the help of Jan-Christoph Tenzer and Daniel Gottschall of IAAT the original software *EPP Tools Suite V.1.5*. was updated to the requirements of the WFI EPP and now allows to display the pixel data which is stored in these files. Since the goal of this thesis was to create a working prototype of the EPP implemented in hardware basic functionality was simulated on a software basis. The emphasis of these tests was put on creating exotic input files, which could probe potential weak spots of the design. Consequently, many of the generated input patterns are unlikely to ever be caused by the observations of the WFI.

PCU The PCU was tested with three sets of input files, containing constant areas with single photon hit patterns, as well as ascending pixel values with each pixel. The main intention of the PCU testing, was to investigate, if the communication with the offset value RAM was working properly and if correct offset values were subtracted from the pixels. **For all conducted tests, the PCU performed as expected.**

CMCU Due to the complex structure of the CMCU, more elaborate tests were conducted to verify its functionality. Since the sorting operation of the CMCU is started with every new line, that has arrived in the unit, input files with alternating line patterns were used in order to see shifts in the file output, if there was an error in the sequence. Also, input files with alternating patterns for both lines and input ports were used, in order to investigate the units behavior for lines consisting of many identical pixel values. **After the adjustment of the internal CMCU pixel counter in correspondence with the VALID_IN signal of the unit, the CMCU handled all input files error free. The calculation of the median for each line was verified, by manually conducting its operations for four test-files and then comparing the results with the simulation.**

ETAU The ETAU was tested with two input files, one containing pixel energy values and one containing arbitrary flag information from the PCU. The main focus of the ETAU testing was set on the correct allocation of flags to the energy values, as well as the synchrony of outputs with the incoming PIXELCLK signal. Simulations of the ETAU revealed, that operations in the unit could not be performed with the currently active input signals, whose change interfered with ongoing operations. Instead a redesign of the EPPs buffering strategy was conducted and which was implemented in all units and buffered each input value, so that processes could operate on "copies" of the signal. **Afterwards, for all conducted tests, the ETAU created the correct flag-patterns.**

PPFU The PPFU was tested with a set of energy values and corresponding flag-patterns. In order to immediately see influences of the unit on the incoming and outgoing data stream, the energy output was set to '0' whenever the incoming flags did not match the filter-mask, while pixels with matching flags were passed through. This method however was only used for testing purposes and later-on exchanged by the setting of the valid-flag for each pixel. **For the conducted test, the PPFU handled all information correctly and only let pixels with matching flag-patterns pass, a behavior which corresponded to the expectations.**

PATSGU The last single unit test was performed with the PATSGU, which creates pixel packages for ground-transfer. The most important aspect, which was investigated in the PATSGU test, was the correct allocation of xy-coordinate pairs to each pixel. For that purpose, an energy value input file was used, while the other inputs like flags and time-stamp were held at constant values. The output file consisted of five columns for flag-pattern, energy value, x-address, y-address and time-stamp. **For the used input file, all pixel coordinates were assigned correctly and connected to their respective energy values.**

CRU Software testing of the CRU was performed in the context of top-level tests of the EPP. Before any software tests of the top-level could be performed, the mode registers of the CRU had to be updated with values representing the respective work-modes of the EPP units, and thus the SPI protocol, as well as the address decoder of the CRU could be tested. In order to simplify the testing procedure, another component, the *SPI-chopper* was developed. Reason for the creation of the SPI-chopper was the serial data transmission of the SPI, which made it necessary to assign every single bit separated by waiting instructions in a test-bench environment. The SPI-chopper however, takes a complete 64-bit SPI signal and writes it to the output, bit by bit, in a serial fashion, thus reducing the amount of source code and work drastically, if a SPI command in a test-bench is altered. It contains a 64-bit input called `DATA_IN`, as well as three further input ports `SYSTEMCLK`, `START_IN` and `SCLK_IN`. Furthermore it features two 1-bit outputs `DATA_OUT` and `ENABLE_OUT`, which are directly routed to the SPI ports `SPI_MOSI_IN` and `SPI_EN_IN` of the CRU. Data, which is read from `DATA_IN` will be stored in a register called `COMMAND_REGISTER`, once the input `START_IN` is set to 'high'. Afterwards, a counter will increase from 0 to 63 with every incoming `SCLK` signal via `SCLK_IN` and write the corresponding register slots of the `COMMAND_REGISTER` to the output `DATA_OUT`. For a count of 0, the chopper will set its output `ENABLE_OUT` to 'low', since it is 'high' by default and serve as an enable signal for the SPI. Once the chopping is completed, all ports will be reset to their default values and the chopper will return to idle mode, waiting for the next signal.

During the software testing period, not all functionalities of each unit were tested. The reason for that is, that most of their respective input signals are generated by previous units, thus making it necessary to create a lot of dummy data and separate input files, which differ for every test-bench. Instead, the EPP was tested as a whole, which limited the amount of manual interventions to a minimum. The only input data needed for the operation of the EPP, were the programming commands of the CRU via SPI, which could be saved directly in the test-bench file, as well as 32768 valid 14-bit energy values, which were stored in a text-file. Equal to the CMCU test-bench, the input files of four tests contained exotic pixel patterns (alternating, ascending, etc.), as well as energies ranging throughout the whole dynamical range of the EPP (refer to Figure 6.2). During the testing of the EPP, it became obvious that the startup of the units had to be handled in the way, which was described in Section 5.2.5. After the timing between all units had been fine-tuned, the EPP handled all incoming data correctly and also generated the correct outputs for energies and flags. Unfortunately, due to limited time, it was not tested yet, if the counting of valid pixels, bad pixels, etc. is working properly. All other aspects of the EPP were investigated for one single frame and could be verified. After reaching this stage in the development of the first prototype, the design was implemented on a Xilinx Virtex-4 SX 35 FPGA.

In the future evolution of the EPP design, systematic and elaborate software testing needs to be performed with a variety of input scenarios in order to probe the EPP's current functionality and ensure its correctness for hardware implementation.

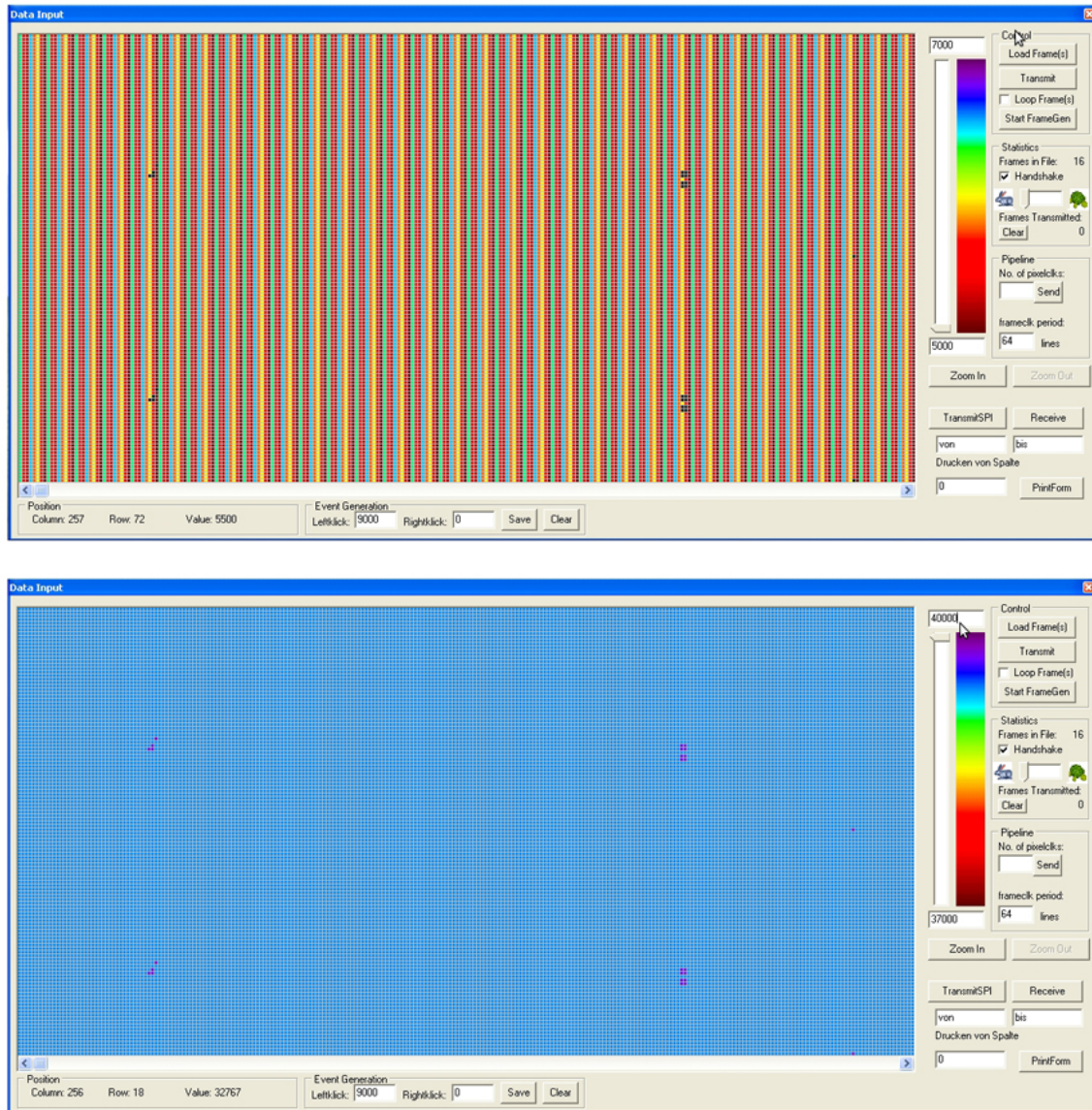


Figure 6.2: Screenshot of a test-bench test result of the EPP with the PCU turned off in order to show the influences of the CMCU only. The top image shows the pixel values and patterns, which were used as input for the EPP. Visible is the alternating line structure with energies ranging from 5000 to 7000 ADU and a few random events with an energy of 10000 ADU. The bottom image shows the same data after it has been processed by the EPP. The dynamical range has been increased by 32768 ADU and the median values have been subtracted from each pixel, making the hit pixels clearly visible.

6.2 Hardware Synthesis

After the successful conduction of various software-based tests of the EPP and its units, the design was synthesized by the Synthesis Tool (ST) of the Xilinx ISE development environment (Version 13.1). At the current stage, the ST renders the design synthesizable at a clock frequency of 159.295 MHz, which is well above the 100 MHz aimed for. Furthermore, the ST currently throws 48 warnings, which are all due to unconnected ports or assigned signals, which remain unused throughout the design. Unfortunately, this circumstance cannot be avoided when aiming for source code, that is well-structured and easy to read. Since warnings are also shown if single bits remain unused, removing all of them would compromise readability and is unlikely to result in an increased maximum clock frequency of the design. Also, some of the unused bits are foreseen to simplify future upgrades of the EPP with new units (for example only 24 of the 32 bits of the LOCALMODE-signal are used at this stage). Due to the time-frame of this thesis, no attempts have been made to improve the overall clock frequency yet. This topic however will be dealt with in Chapter 7.

After the design completed the PAR stage, it was loaded into the PROM of the FPGA and mounted on the *D3C Performance Verification Board 1.6* (DPVB), which was designed by Jürgen Dick of IAAT and can be seen in Figure 6.3. This board does not only host the Xilinx Virtex-4 SX 35 FPGA, but also a *USB Interface V2.5* which was manufactured by *BrainTechnology Home Automation*¹ from Westerfeld, Germany. The USB module serves as an interface between the EPP Tools Suite V.1.5. software by Jan-Christoph Tenzer and the EPP. The software will generate SPI input signals, which are transmitted via USB and then routed to FPGA input pins by the USB module (via the SPI2 connection pad on the DPVB). In the constraints-file of the VHDL design, these input pins are assigned to the SPI communication pins of the CRU and thus allow handling SPI communications with the EPP via computer. For this purpose, Daniel Gottschall of IAAT adapted the *Controller Pane* of the software to the 64-bit SPI implementation. Two text-input fields for hexadecimal values of address and data are provided and can be used in read or write mode via the send- and receive-buttons. Within the EPP top-level, a process called `displayReceiveSPI` will switch on two LEDs (D3 and D4) of the DPVB for about 1 second for every commenced SPI transmission. In order to synchronize the SPI clock signal (SCLK) with the SYSTEMCLK of the EPP, the SCLK provided by the USB module, was used as a GCLK input for the EPP (pin AF12 of the FPGA and CLKOUT on the USB module). Due to the fact, that the EPP is currently only operated with a clock frequency of 48 MHz and that the SpaceWire Interface used for data transfer to further periphery is not yet implemented in the EPP, no performance critical hardware-based testing could be performed. Instead, general functionality of communication via SPI was tested and enabled write and read operations of the CRU's RAMs and registers via software.

6.2.1 Hardware Diagnostics

The DPVB offers a bank of pins just below the FPGA socket, which can be mapped with internal signals from the VHDL design. In case of the EPP, this bank was used in order to route internal control signals to the pins on the outside, where they can be checked and

¹<http://www.braintechnology.de/braintechnology/>

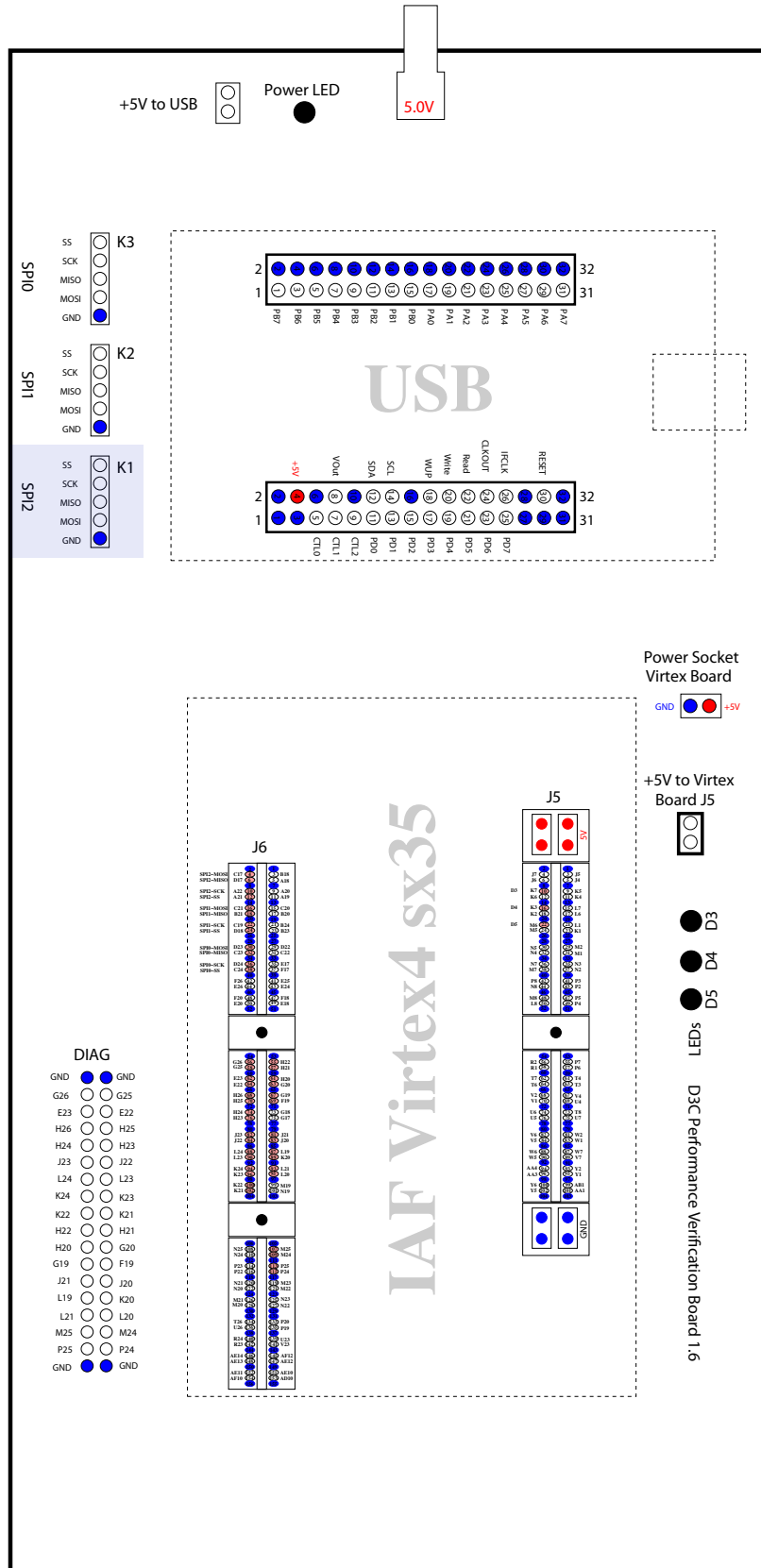


Figure 6.3: Schematic of the D3C Performance Verification Board 1.6 by Jürgen Dick of IAAT. The right socket will host a USB Interface V2.5 by Braintechnology and use the SPI2 output (marked blue) for communication with a Xilinx Virtex-4 SX 35 FPGAs, which is mounted on the left socket. Image by Thomas Schanz of IAAT.

Table 6.1: A list of all current signals routed to external diagnosis pins on the DPVB, as well as their corresponding FPGA connection pins, their I/O type and a short description of their functionality.

Signal name	FPGA pin	IO Type	Description
CLK	AF12	Input	global clock in from USB module
CLK_OUT	G26	Output	control pin for CLK signal
PIXCLK_OUT	P25	Output	control pin for PIXELCLK signal
EPP_OSZI_OUT	A12	Output	simple connection test signal
EPP_TEST_OUTB<0>	K7	Output	LED D3 on the DPVB
EPP_TEST_OUTB<1>	K3	Output	LED D4 on the DPVB
EPP_TEST_OUTA	M6	Output	LED D5 on the DPVB, CLK signal
EPP_SCLK_IN	A22	Input	SPI clock signal
EPP_EN_IN	A21	Input	SPI enable signal
EPP_MOSI_IN	C17	Input	SPI data input signal
EPP_MISO_OUT	D17	Output	SPI data out signal
EPP_LED_ROT	F14	Output	red LED on the IAF Virtex Board
EPP_LED_GELB	F13	Output	yellow LED on the IAF Virtex Board
EPP_LED_GRUEN	F12	Output	green LED on the IAF Virtex Board
EPP_LED_BLAU	F11	Output	blue LED on the IAF Virtex Board
EPP_IOSIG_TEST	E23	Output	SPI "IO signal read" complete pin
EPP_ADDRESS_TEST	E22	Output	SPI "address read" complete pin
EPP_DATA_TEST	H26	Output	SPI "data read" complete pin
EPP_VALID_OUT	H20	Output	valid output data control pin
EPP_START_IN	G20	Input	valid input data control pin

investigated with the help of oscilloscopes and logic analyzers. A table of these signals, as well as their corresponding output pins is given in Table 6.1. Currently, the most noticeable diagnosis tools are the red, yellow, green and blue LEDs on the IAF Virtex module. Each of them is assigned to display the current LOCALMODE of one of the central units of the EPP. The red LED is assigned to the PCU, the yellow one to the CMCU, the green one to the ETAU and the blue one to the PPFU. Their respective blinking mode in reference to LED D5, which blinks once every second for 48 MHz of clock frequency of the FPGA, will denote which LOCALMODE the single units are currently switched to. For the two main modes stop and work, the LEDs will be turned off or on permanently. If a unit is switched to bypass-mode, its respective LED will blink in-phase together with LED D5, which checks if the internal SYSTEMCLK signal is working properly. If some other command is written into the CRU's LOCALMODE_REGISTER, which cannot be interpreted by the case structure of the displayMode process, the LED of the respective unit will blink out of phase with D5, thus denoting that no valid LOCALMODE was selected. Consequently, the four LEDs will offer a fast way to investigate the functionality of the SPI, when it is writing into the LOCALMODE_REGISTER, as well as the interpretation of the corresponding signal by four of the EPP's units.

6.3 Results

As already described in Section 6.1, the functionality and performance of the current EPP design could be verified by conducting a number of software-based test-bench simulations, which showed, that the EPP is capable of handling the required amount of data and that its processing capabilities are more than sufficient to perform tasks according to the WFI specifications. Time-critical processes like the sorting of pixel lines, as well as the analyses of thresholds and pixel positions, could be performed with the help of a pipelined design structure and innovative implementation of parallel sorting algorithms. In fact, the OETS algorithm has been implemented in hardware for the first time at the IAAT in the framework of this thesis. All units were tested as standalone units as well as being interconnected and allowed testing of their memories and communication with each other. The testing also revealed, that the EPP conducts its tasks correctly and that it will be able to flag valid event pixels for further processing. During this investigation, test-bench simulations proved to be an important asset in pre-synthesis functionality and performance analysis and helped to realize different testing scenarios. Also, the text-input and -output capabilities of VHDL enabled the conduction of different tests, which were already described for each unit. It has to be noted, that the current EPP design is already very mature, even though a large portion of development time was dedicated to creating test-setups and conducting simulations and hardware measurements.

Concerning the hardware implementation of the EPP, a first working prototype was fabricated in the framework of this thesis. With the results from the software test-bench and the results from the ST, it can be assumed, that the EPP will handle incoming data correctly, if it is provided in a correct format and with correct timing. During the last weeks of this thesis, extensive hardware testing concerning the SPI data transmission was performed and its correct functionality could be verified (see Figure 6.4). With the implementation of the USB module on the DPVB, it was possible, to utilize the already existing EPP communication software, in order to write and read data from the EPP's RAMs and registers. Furthermore, the correct functionality of the LOCALMODE control could be verified for four units of the EPP. Since all units implement the same processes concerning their working modes, it can be assumed, that this feature is operational in all units of the EPP already. The only error during the SPI communications testing occurred when trying to read all values stored in the offset LUT of the PCU. For all tests, one or two pixels of the WFI stripe were read out incorrectly by the software. This phenomenon however, could only be observed, if all pixels of the stripe were selected for readout. When reading out corresponding single pixels, which were incorrectly readout during full-readout, the values read from the LUT were correct. It is therefore highly unlikely, that this error is due to a erroneous function of the EPP, but due to the software controlling the readout procedure or the signal submitted by the USB module. Further investigations need to be performed in this area however, to ensure the correct and stable operation of the USB module for further hardware-based testing.

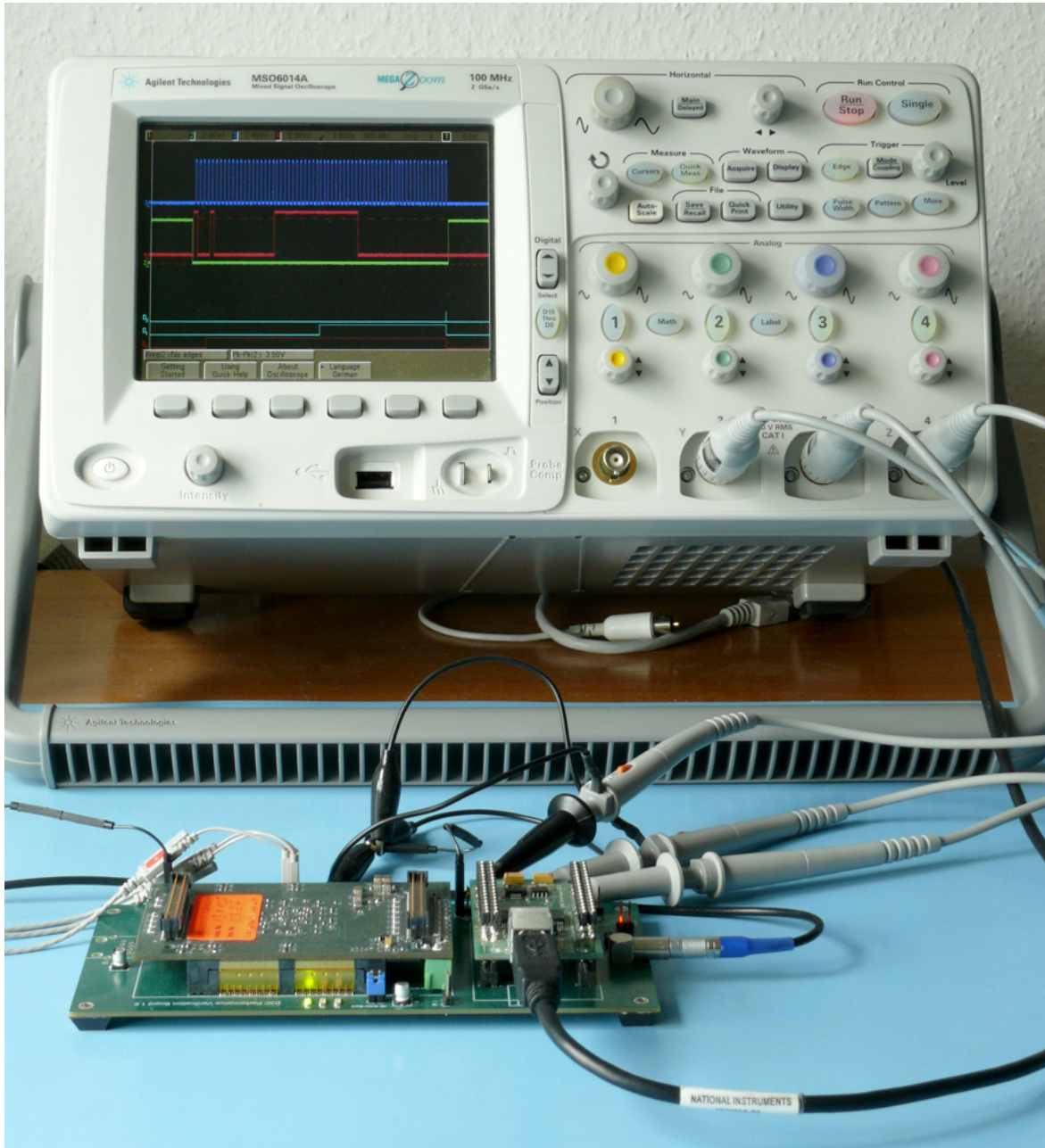


Figure 6.4: Photograph of the first EPP prototype, being investigated with the help of a combined oscilloscope/logic analyzer. Since the probes of the oscilloscope are connected to the SPI2 port of the DPVB, the signals on the screen show, that SPI data is transferred from the computer via the USB module into the FPGA. The blue signal shows the EPP_SCLK_IN signal, while the green and red signals show the EPP_EN_IN and EPP_MISO_IN respectively. During the 64 SCLK events, the SPI protocol transmits I/O-mode "0001" (input), address "xFFF0001" (LOCALMODE_REGISTER) and data-value "x000001FF" (work-mode for PCU and CMCU, bypass-mode for ETAU and stop-mode for PPFU, PATSGU and TDGU).

7 Summary and Outlook

7.1 Further Design Implementations

As already mentioned in the previous chapters, the current EPP design represents a very mature first working prototype, but is still not completely implementing all aspects, which were defined by the WFI instrument working group. The reasons for that are the limited time-frame in which this thesis had to be concluded, as well as the lack of concrete specifications for some aspects of the WFI and the corresponding electronics. Whenever possible, groundwork for future implementations was laid in the current EPP design in order to simplify updates in the future. The following section will focus on some aspects, which are likely to be added to the current design after this thesis is completed.

7.1.1 Window Modes

The design of the WFI aims at the implementation of a so-called window-mode readout scheme, where only parts of the WFI detector are read out, but at an increased frame-rate. At the current stage of the thesis it was not clear yet, if these windows are confined to one single WFI sector or if they can be spread over multiple sectors. A complete implementation of this function was therefore impossible. Assuming, that each window will have a starting row and a width however, the two registers `WINDOWSTART_REGISTER` and `WINDOWWIDTH_REGISTER` have been added to the CRU and were equipped with dedicated output ports, that can be connected to any unit in the EPP pipeline, which needs the corresponding information. Depending on the final setup of the window mode, the counting processes in the EPP will have to be adjusted in order to switch counters back to the corresponding starting pixel number (`WINDOWSTART_REGISTER`), if the end of a window is reached (currently all counters count from 0 to 64).

7.1.2 Linear Gain Correction

In addition to the offset correction of the PCU, the final version of the EPP will also implement a linear gain correction for each pixel. Due to the fact that the DEPFET is an APS and implements a FET structure for each pixel, it will amplify the influence of the signal charges intrinsically. Small fabrication variations in the geometry or homogeneity of the readout node however, will cause variations in the corresponding amplification, thus requiring a separate gain-factor for each pixel. The storage of these gain-factors is already foreseen in the CRU, where addresses for SPI communication have been reserved in hex group `0x002` and `0x003`. The current idea is to implement the gain correction after the pixels have passed the CMCU. Since the corresponding unit is also a pixel value correction unit, it will be called PCUB, while the PCU will be renamed to PCUA.

7.1.3 Creating a Time-Stamp

Until now, the exact implementation of the time-stamp reset mechanism for the EPP is still unclear and also the interval in which resets will be conducted is not yet specified. As a consequence, currently a 28-bit counter is foreseen which will overflow every 2.68 seconds at a SYSTEMCLK frequency of 100 MHz. The current time-stamp process `setTimestamp` does not consider an external EPP time-stamp reset input yet, but sets back its count once the maximum count is reached. As soon as the design of the WFI sequencer and readout electronics is finalized, the reset function can be implemented.

7.1.4 Threshold Values

The PCU and ETAU of the EPP pipeline perform a series of event threshold analyses, where they utilize threshold values stored in the CRU. At the moment, these default values are just arbitrary values, which are not based on valid scientific assumptions, but only on ad-hoc considerations. Future designs of the EPP should therefore store realistic values in the corresponding registers. The update of threshold registers via SPI however is already implemented and possible during EPP operation.

7.1.5 Common-mode Correction Refinements

The current implementation of the common-mode correction in the CMCU is based on finding the median of all pixels of a line. If these lines contain a lot of bad pixels or pixels which are marked as MIP events, the median value can be compromised. In order to cope with such situations, current planning foresees to exclude bad or MIP-flagged pixels from the median determination. The exact way of how to achieve this functionality is not clear yet, however the fact, that not all 196 available SYSTEMCLK events are needed to complete the sorting of one row and the fact that the reduction of elements in a row will also reduce sorting time, offers leeway for the implementation of this feature.

7.1.6 Fiber Optics Connection Unit

Additional to the PATSGU, which handles the preparation of pixel-data for ground transfer, another unit will be needed in order to pass on data to the following electronics. This *Fiber Optics Connection Unit* (FOCU) will format data coming from the PATSGU in a way, compatible with a not yet defined fiber optics data protocol. The exact implementation specifications are currently still not finalized, thus rendering the design of the unit not feasible at the moment. For performance testing purposes however, the implementation of the *SpaceWire* protocol, which is a fast data-transfer interface commonly used on satellite-based missions, should be added to the roadmap of further EPP evolution.

7.1.7 Principle Optimization Efforts

The current design of the EPP represents a first working version and has only partially been optimized in terms of CLB usage and process structures. It is likely, that many of the EPP's current operations could also be implemented by processes, which are structured in a different way than current ones ("there is more than one way to do things"). Reducing the level of

abstraction in VHDL processes and explicit utilization of so-called primitives, could further improve the device's maximum clock frequency, even though it already excels its requirements. Furthermore, settings of the Xilinx synthesis tool can lead to improved clock frequencies, since options like resource-sharing and optimization effort for example, can be adjusted manually and save CLBs of the FPGA. Improvements in this area could lead to an increase of the EPP's data-handling performances, thus allowing ever higher frame-rates than currently foreseen.

7.2 Software Testing and Evolution

It was already mentioned, that software-based testing of the EPP was performed with the help of test-benches. In the process of this design-step, single units as well as the interconnected pipeline were investigated. Of course the tests, that were performed in the context of this thesis could not cover all possible aspects of the EPP's functionality. Nevertheless, their results lead to an increased confidence in the correct function of the EPP. In future stages, thorough and systematic software tests using exotic pixel patterns and energies should be conducted in order to rule out possible design errors. These tests should have systematic characteristics and gradually probe the limits of the EPP's performance. Additionally, tests with realistic pixel data should be run as well. Data obtained from simulations or other pixelated photon detectors could be used in order to prove, that the EPP will operate as expected under normal conditions, thus completing the possible data-input scenarios. With new implemented aspects like window-modes, etc., corresponding tests will have to be designed and performed as well. Aside from investigating the correctness of the EPP's functionality, further testing is likely to lead to improvements of the design. Whenever an error occurred during the software testing phase of the current EPP version, it usually also lead to an improved design in terms of CLB usage and maximum clock frequency. In general, a lot of times the refinement of the device goes hand in hand with extensive simulation, thus rendering it an effective way to push the limits of the electronics.

Lastly, software testing should be conducted with huge amounts of artificial pixel data in order to investigate the EPP's performance under full occupation and probe the correct counting of pixels and resetting of registers across frames, before moving on to more extensive hardware-based testing.

7.3 Hardware Testing and Evolution

One very important aspect of future hardware testing will be the hardware-based verification of correct data-handling of the EPP. Since this aspect could not be verified in this thesis, it is essential to investigate it in the future evolution of the EPP. In principle, it should be achieved in two steps. In a first stage, large amounts of artificial pixel data should be inserted into the EPP pipeline via the EPP Tools Suite V.1.5. and then fully processed. In order to conduct meaningful tests concerning the EPP's performance, the FOCU needs to be implemented and the EPP needs to be connected to the chosen fiber optics interface. Hardware for SpaceWire-based data transfer already exists at the IAAT and could be used for reading the EPP's output data directly into a computer. Not only could the correct functionality of the EPP be verified that way, but also first performance critical testing could be conducted and it could be checked if the pipeline can really handle 1000 frames per second.

In a second step, the EPP should be implemented in the setup of a real detector. The WFI science verification model for the XEUS mission, which was set up and characterized by Dr. Michael Martin of IAAT, could serve as a first basis for further testing of the EPP and involved electronics and the interplay between the EPP and the sequencer for the WFI. Figure 7.1 shows the current floor plan for WFI electronics and emphasizes the importance of correct interplay and timing between all involved electronics, due to their complexity and modularity.

A final test and implementation of the EPP will only be conductible, once a final selection for the readout electronics for the DEPFET matrices has been made. At the moment, the VELA ASIC is foreseen in the electronics layout, but its final specifications are currently unknown. In a best-case scenario, the HLL of MPE can supply the IAAT with a 128 x 128 or 256 x 256 DEPFET prototype with VELA ASICs for implementation in the current Simbol-X LED test setup in the near future.

7.4 Current Status of the IXO Mission

In a 2010 released decadal survey by the US National Research Council the organization suggested a continued cooperation of NASA with ESA, while at the same time ranking all three L-class missions, which were proposed in the CVP framework highly, but not at first priority. As a consequence, it became quite unlikely, that the foreseen timetables for any of the three missions could be fulfilled. In order to progress IXO in the future, the *Science Programme Committee* (SPC) of ESA proposed a drastic redesign of IXO and its hosted instruments and science goals, in order to be able to launch the mission led by ESA - in a worst-case scenario even without the help of NASA - in the original timeframe, which proposed a mission start in 2020. Furthermore they set February 2012 as a target date for presenting a new and updated IXO proposal to the SPC. The goal of the restructuring effort was set to conserve essential parts of the science goals, while at the same time reducing cost considerably (approximately 800 Mio. Euro). It has to be noted however, that SPC still advocates a US and Japanese involvement, if they decide to support its efforts in the future. For that purpose - as NASA recently published - the current NASA IXO teams will not be disbanded immediately but will try to redirect NASA's efforts in the context of the recommendations proposed in the decadal survey. Funding for the IXO science team is continued through *Fiscal Year 11* (FY11). (Favata, 2011), (White and Bookbinder, 2011)

Until now, no redesign proposals have been published, making it impossible to foresee the future of the WFI and therefore the future of the EPP development for this instrument. As already mentioned in the earlier chapters however, many aspects of the current EPP design can be applied to any pixelated photon detector, thus making them independent of a specific mission. Newly implemented aspects, such as the OETS are fundamental tasks in hardware-based data analysis and can be used for future mission designs as well. The work done in this thesis therefore remains mostly untouched by the outcomes of any decision on IXO and furthermore enlarges the current knowledge of the IAAT hardware group.

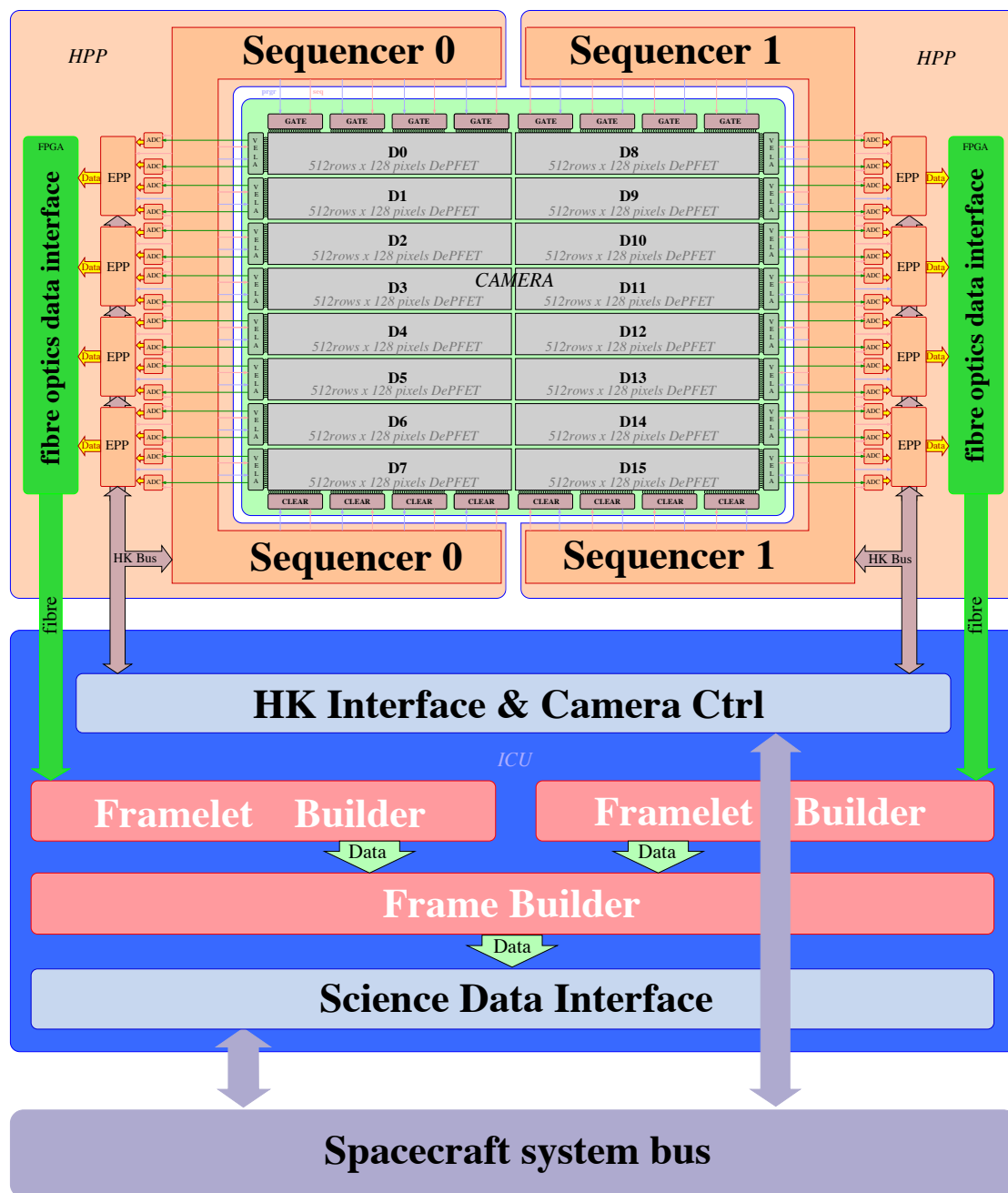


Figure 7.1: Floor plan of the WFI's electronics. Shown are the two hemispheres of the WFI, as well as their separate electronics, which are grouped in a so-called *Hemisphere Pre-Processor* (HPP). Each HPP contains four EPPs, which communicate with a fibre optics data interface. Data received from the EPPs is transferred to electronics, which will build a framelet out of the pixel data, which is merged to a frame after a pixel-pattern analysis. The frame will finally be written to a *science data interface* and transferred to the *spacecraft system bus* via SpaceWire. From the last stage it will be sent to the ground-based control center. Image courtesy of Thomas Schanz, IAAT

7.5 Summary

This thesis has been centered around the hardware-based analysis of pixel data created by modern day pixelated photon detectors. Due to their creation of large amounts of data, even for short-timed observations, it is necessary to preselect scientifically relevant events from the raw-data stream onboard satellite based missions. The current design of the EPP is an evolution and upgrade of the pre-existing D3C EPP design by Thomas Schanz and allows a thorough realtime analysis of these data sets, even at very high frame-rates. It implements new operations like the common-mode correction in innovative new ways and makes extensive use of the parallel processing capabilities of FPGAs. All design steps for modern-day electronics design with HDLs have been completed in the framework of this thesis and have led to a first working hardware prototype. The short time-frame, which was available to conclude these steps once again stresses the importance of FPGAs in electronics development. All work was conducted with already existing hardware, thus reducing development cost to a minimum. The possibility to simulate the electronic's behavior on a computer prior to its synthesis, proved to be a very important tool for debugging and created a strong confidence in the EPP's correct functionality and performance.

With its already very high maturity, the EPP represents a strong basis for future developments at IAAT and many aspects of its design are likely to be transferred to electronics for other missions as well. Its modularity and clear structure allow for simple upgrades and extensions of the involved units and lay the groundwork for further development in the future.

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Erklärung

Hiermit erkläre ich, Stefan Dennis Christmann, geboren am 06.10.1983 in Koblenz/Rhein, dass ich meine Diplomarbeit mit dem Titel "**Design and implementation of an FPGA-driven, hardware-based realtime data reduction system for pixelated photon detectors**" selbständig verfasst und nur die in diesem Dokument angegebenen Quellen und Hilfsmittel verwendet habe.

Tübingen, den 10.06.2011