A FAST ONE-CHIP EVENT-PREPROCESSOR AND SEQUENCER FOR THE SIMBOL-X LOW-ENERGY DETECTOR

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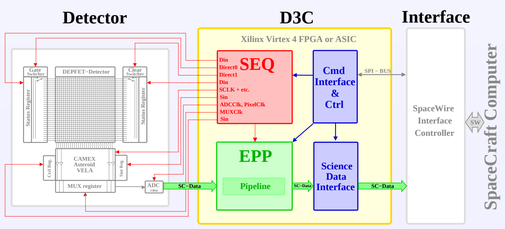
Introduction

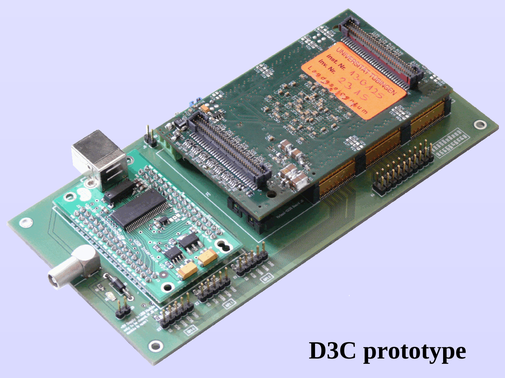
We present an FPGA-based digital camera electronics consisting of an Event-Preprocessor (EPP) for on board data preprocessing and a related Sequencer (SEQ) to generate the necessary signals to control the readout of the detector. The device has been originally designed for the Simbol-X[1] low energy detector (LED). The LED[2] is a 128 x 128 pixel DEPFET (Depleted P-channel Field Effect Transistor) matrix provided by MPE[a] and MPI-HLL[b] and will cover an energy range of 0.5 to 17 keV. The EPP operates on 64 x 64 pixel images and has a realtime processing capability of more than 8000 frames per second. The goal of our current work is to combine the already working releases of the EPP and the SEQ into one single Digital-Camera-Controller-Chip (D3C) until the end of September 2009.



[a] Max-Planck-Institut für extraterrestrische Physik - Garching, Germany
[b] Halbleiterlabor des Max-Planck-Instituts, München - Neuperlach, Germany

The D3C Setup

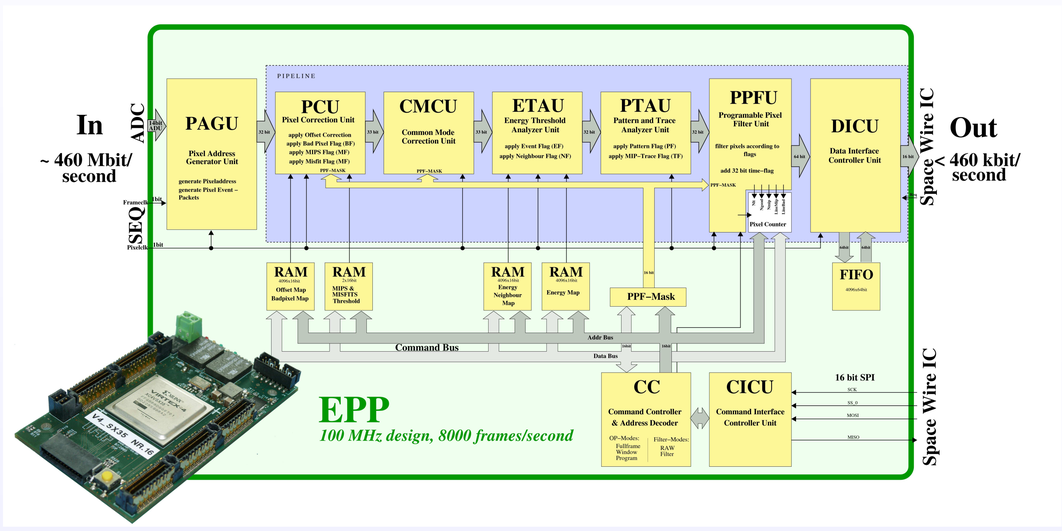
The D3C is a Xilinx Virtex-4 FPGA based design, written in VHDL. Later on, it can be easily adapted for a radiation hard ASIC technology or benefit from Xilinx' recent release of the Virtex-4QV FPGA family, a space qualified version of the Virtex-4 FPGA. The high readout and processing speed of the EPP is accomplished by a multistage pipeline concept and requires a base clock frequency of 100 MHz. Currently, the EPP is designed to process lines of 64 pixels; future releases may also operate on 128 pixels or more. The EPP input is connected in parallel to a 14bit ADC. For each pixel, the EPP performs an offset- and common-mode correction, adds pixel coordinates and a time tag, analyses and filters pixel energies against certain energy thresholds and performs a pattern analysis. At its output, only valid events leave the processor, resulting in efficient data reduction depending on the chosen parameters. The EPP-output can be connected to an interface controller (IFC), enabling a SpaceWire connection to the spacecraft bus. The sequencer (SEQ) generates all necessary digital control- and programming-signals to propel the readout- and SWITCHER-chips of the DEPFET-matrix or a pn-type CCD-detector.



D3C prototype

The Event-Preprocessor Design

The high processing speed of the EPP requires a multistage pipeline concept. The input data of the EPP is a 14 bit wide bus which contains the energy of each of the 4096 pixel for each frame, resulting in a constant data stream of about 460 Mbit/second. At the end of the EPP-pipeline each pixel contains information about the energy (14 bit), the position (12 bit) and a time tag (32bit). Only valid pixel will pass the EPP pipeline.

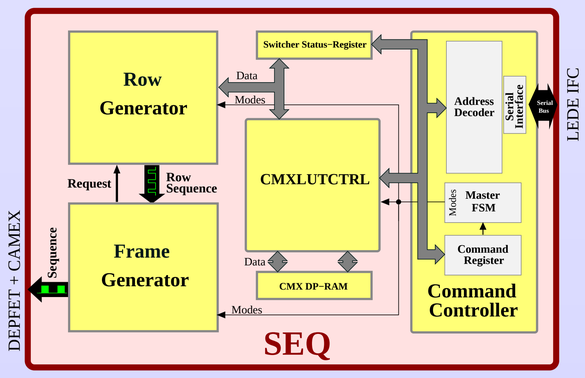


The main purpose of the EPP is data reduction and correction. Several tasks are implemented into the EPP design. Its modularized structure reflects the order of operations that are applied sequentially on the data:

- **offset correction:** An offset value for each pixel is stored in a Look-Up-Table (LUT) and can be subtracted from the individual pixel energy (PCU). The offset-LUT also contains a bad pixel flag for each pixel. The LUT can be calculated on board or uploaded from ground.
- **MIP/misfit rejection:** Minimal ionizing particles (MIPS) can be detected by utilizing a programmable high energy threshold, common for all pixels. The so flagged pixels can be rejected inside the EPP event filter. Misfit events occur, when photons hit a pixel during the readout procedure. In this case a negative value of the pixel amplitude may occur. Misfits are also flagged and can be rejected (PCU).
- **common-mode correction:** Small variations of the supply voltage of the CAMEX readout chips cause notable variations in the pixel amplitudes. The effect concerns all pixels of a line simultaneously. This common-mode noise can be effectively removed by the EPP with a filter (CMCU), where the median value of all pixels of a line is subtracted from the pixel amplitudes. In order to obtain the median in realtime we invented a highly parallel hardware based routine which can process the median of 64 pixels in less than 2 μs.
- **energy filter:** The energy of each pixel is compared individually to an upper and lower energy threshold (ETAU). Pixels adjacent to such a valid pixel will be compared to a separate Neighbour Pixel Threshold.
- **valid pattern recognition:** Electrons generated by an incoming photon can be spread over more than one pixel if the event occurred near a pixel border (split events). The valid event patterns that can result from this process will pass the Event-Preprocessor, other connected pixel will be rejected and filtered out. For this task we invented a very fast hardware based pattern filter pipeline (PTAU) that can perform a pattern analysis for each pixel in less than 30 ns.
- **event filter:** The event filter of the EPP (PPFU) is programmable by ground station and can reject invalid events for further transmission to ground. Valid events must meet all the following requirements:
  - pixel amplitude is above a lower threshold (ETAU)
  - pixel is not flagged as bad (PCU)
  - pixel is not a MIP event, adjacent to a MIP event or a misfit event (PCU)
  - pixel belongs to a valid pixel pattern (PTAU)

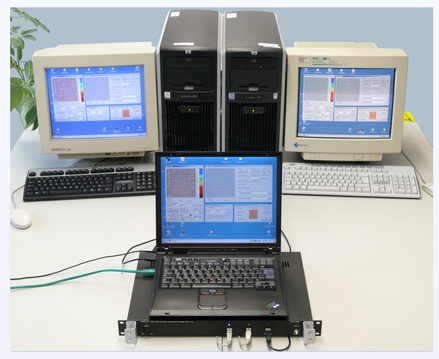
The Sequencer Design

The purpose of the sequencer is to supply all vital parts of the camera with digital signals in order to control the operation and the readout of the detector. A total of 38 different configurable signals is generated for each quadrant. Besides driving the readout, some signals are also necessary to program the registers of the CAMEX- and the SWITCHER-chips, which control the mode of operation of the camera. Finally the SEQ-design will be merged with the EPP-design into one chip, the D3C.

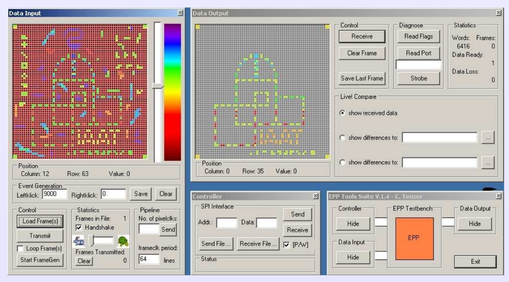


EPP Testbench

In order to verify the function of the EPP we have developed a hardware testbench in our electronics lab. All functions of the EPP were successfully verified with this function verification testbench during 2008. Meanwhile, we have extended this setup to a full working performance verification environment. For the time being, the EPP is thoroughly tested with this setup under realtime condition with a continuous input data stream of 460 Mbit/second corresponding to a frame rate of 8000 frames/second.

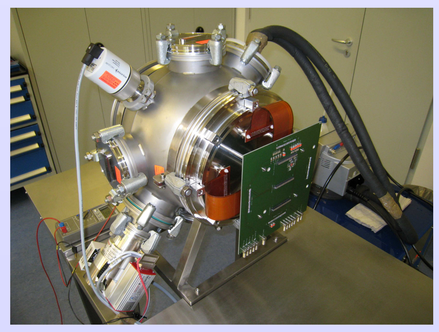


The picture below shows a screenshot of the EPP-Testbench-Software. The software can generate artificial detector data as well as load real detector raw data (e.g. from a 64 x 64 pixel DEPFET matrix) and feed it into the EPP. Another part of the software can visualize the EPP output and compare it with the input data. A third part of the software performs the commanding of the EPP. The testframe shown in the picture contains the IAAT-logo as artificial input data. On the left side is the input frame with several distortions, on the right side is the filtered output of the EPP.



SVM Testchamber

The following picture shows the Science-Verification-Model (SVM) setup for Simbol-X in our lab. Its purpose is to operate a quadrant of the LED together with one camera module of the CdTe high energy detector[3] in a vacuum environment at -40°C. In the first stage the setup will be operational with only the LED, the EPP and the SEQ installed at the end of June 2009.



[1] P. Ferrando et al. *The Simbol-X mission*, MmSAI, v.79, p.19 (2008)
[2] P. Lechner et al. *The low energy detector of Simbol-X*, Proc. SPIE, v.7021 (2008)
[3] A. Meuris et al. *Caliste 64: detection unit of a spectro imager array ...*, Proc. SPIE, v.7021 (2008)

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