Eberhard Karls University Tübingen
Department of Physics

MASTER THESIS

An ASIC-Simulation Board for the EUSO superpressure balloon

by

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Abstract

JEM-EUSO is a large UV telescope that will be deployed on the International Space Station to observe fluorescence light produced in extensive air showers in order to detect ultra high energy cosmic rays.
The EUSO Super Pressure Balloon (EUSO-SPB) serves as a pathfinder mission for the EUSO program by using the same hardware components for its flight.
The Institut für Astronomie und Astrophysik Tübingen contributes to this project with the development of the Photo-Detector Module (PDM) and the Cluster Control Board (CCB), which are both essential parts of the focal surface electronics.
This master thesis is devoted to the development of an ASIC-Simulation Board (ASB) with a ZYNQ 7000 SoC as the core component, to allow hardware testing of the PDM and CCB in absence of the original SPACIROC ASIC. It also includes the implementation of an upgraded First Level Trigger algorithm for the PDM as well as the design of a small adapter board in order to enable to utilize the ASB for project unrelated applications.
While the First Level Trigger version of this thesis has been used for the final integration of the EUSO-SPB instrument, the ASB has been completed and tested in a laboratory hardware setup.

Introduction

The Extreme Universe Space Observatory on a Super Pressure Balloon (EUSO-SPB) is a cosmic ray experiment, designed to detect fluorescence light from ultra-high energy cosmic rays (UHECRs) by looking down from above the atmosphere. The experiment evolved from the JEM EUSO project and represents a further development of the EUSO-Balloon mission, which was succesfully launched in August 2014 and collected data for five hours[1].
The JEM-EUSO program was originally a mission attached to the Japanese Experiment Module of the International Space Station (ISS) consisting of an UHECR telescope and an atmospheric monitoring device.
The EUSO-SPB will be the first experiment to detect the UV light from UHECRs from above and also may be able to observe the Cherenkov radiation of these particles. Besides this main scientific objective, EUSO-SPB will also monitor the atmosphere for further UV signals with pulse like characteristics as transient luminous events (TLEs), localised-surface-plasmons (LSPs)and measure the continuous variation of UV light from airglow[2].
The onboard instrument consists of an updated version of its predecessor, the EUSO-Balloon with one JEM-EUSO Photo-Detector Moudle (PDM), and an optical system consisting of three Fresnel lenses with a field of view of six degrees. Unlike during the EUSO-Balloon mission the updated trigger implementation will now allow to read out and process cosmic ray events.
The EUSO-SPB mission was launched in April 24th 2017 from Wanaka (New Zealand) and landed on the South Pacific Ocean on May 7th. The Data analysis is currently in process.

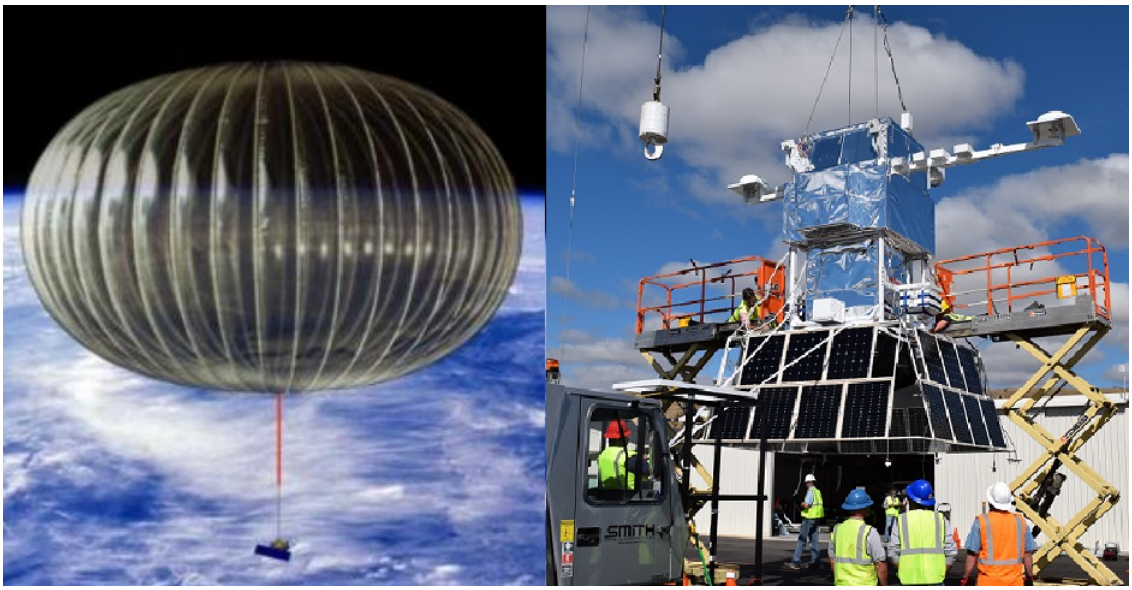


Figure 1 – The EUSO Balloon shown at the left, the mechanical structure of the telescope in Wanaka shown at the right. Images: [63]

The Institut für Astronomie und Astrophysik (IAAT) provided the Photo-Detection Module (PDM) and the Cluster Control Board (CCB), which are both essential parts of the focal surface electronics and for the hierarchical trigger scheme and was therefore responsible for the necessary changes of the trigger implementation. This master thesis contributes to this improvement by providing an ASIC-Simulation Board (ASB), which allows to test the VHDL implementation on the PDM in the absence of the original ASIC board, which is responsible for reading out of the Multi-Anode Photon multipliers (MAPMTs).
The development of the ASB includes the design and manufacturing of a carrier board, as well as the hardware and software implementation on an ZYNQ SoC platform. The Board is

capable of receiving simulation data from a PC and sending it to the PDM according to the bus protocol of the original ASIC. In addition the ASB is able to serve as a development board for project unrelated applications. For this task a small adapter board has been developed, which allows the free use of 64 Inputs/Outputs.
The master thesis also includes the implementation of an optimized version of the First Level Trigger (FLT) on the PDM, which has been utilized for the final instrument integration.

Section one gives a in depth description of the science objectives of JEM-EUSO and the phenomena that are expected to be observed. An Overview of the missions which emerged from the JEM-EUSO project is given in section two.
Section three describes the architecture and function of the JEM-EUSO instrument, while Section four shows the functionality of the instruments trigger system and the implemented changes of the First Level Trigger.
The design of the ASIC Simulation Board with its hardware architecture and programming is described in Section five followed by an overview of the test results (Section six).
A conclusion and a short outlook about possible future projects utilizing the ASIC-Simulation Board is given in Section seven.

Contents

1 Science objectives

The JEM-EUSO program was set up to address fundamental questions of high-energy astrophysics by exploring the origin of cosmic rays at energies above 5×10^{19} eV. 100 years after their discovery by Victor Hess, cosmic rays are still poorly understood, as their origin, and their production mechanism, as well as their propagation through the intergalactic medium remain uncertain. In theory only very few astrophysical sources have the ability to accelerate particles to the most extreme energies of 5×10^{20} eV or 10 J. Also the extremely low flux of only a few particles per km^2 per year at the highest energies complicates the detection of an sufficient amount of events calling for the need for extremely long exposures.
The largest operating experiment so far is the Pierre Auger Observatory located in Argentina, which detects particles within an area of 3000 km^2. In order to achieve better statistics developing ground based Observatories exceeding the magnitude of Auger prove to be very difficult, observing CRs from space is a logical step as the observational area for JEM-EUSO with 1.4×10^5 km^2 is an order of magnitude larger than that of Auger.
As the EAS will be observed from above the atmosphere, EUSO-SPB will not only be able to detect more rare UHECR events than ground based observatories, but can also play a role in the research of further UV phenomena of the Earth's atmosphere like LSPs, TLEs and meteoroids[3].

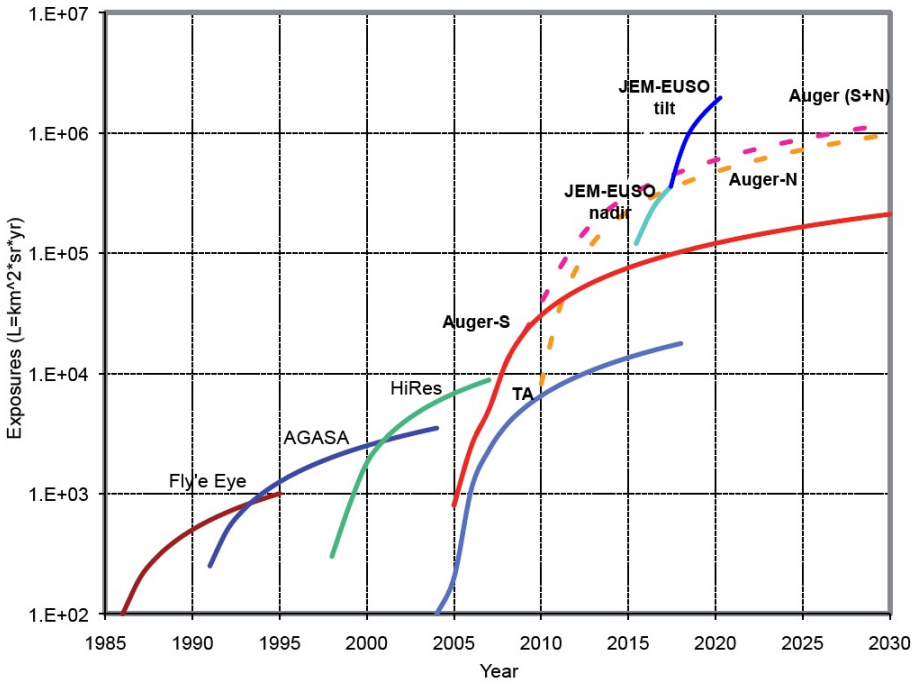


Figure 2 – The expected cumulative exposure of various experiments in km^2 sr and yr. The turquoise curve shows the exposure in pure nadir mode, while the blue curve corresponds to pure tilted mode of JEM-EUSO, which has a higher expected exposure than all other experiments including the postponed Auger North project. The tilted mode increases the observational area and the distance between EAS and instrument and therefore increases the energy threshold compared to the nadir mode. Image: [63]

1.1 Ultra high energy cosmic rays

The following section is based on Mészáros (2010) [29] and Longair (2011) [6]. Cosmic rays are particles with high energies propagating through space. The range of energy and flux extends over a huge span beginning from 10^8 eV up to 10^{21} eV with the corresponding flux from more than 10^5 m^2 particles per second to less than one particle per km^2 per millennium. Their composition at energies between 10^8 and 10^{10} eV consists of Protons (86%), Alpha particles (11%), Electrons (2%) and heavier elements (1%).

At energies below 10^{10} eV the particles are still influenced by solar activity and gain a time dependent feature anti-correlated to the solar cycle, which is called solar modulation. This phenomenon appears due to the outflowing Solar wind diffusing the cosmic ray particles on their way from interstellar space to the Earth. The disturbances of the interplanetary electromagnetic field, which interferes with particles with energies less than 10^9 eV on their propagation to Earth increases with the solar activity. The solar model can be characterized by a diffusive-convective model in which the magnetic perturbations in the Solar wind scatter the particles [30].

For higher energies the particles start to be independent from the sun's activity as they behave more rigid to external magnetic fields. From this energy the spectrum follows a declining power-law: $\frac{dN}{dE} \propto E^{-q}$ with an index of $q \sim 2.7$ up to 10^{15} eV.

At this point a feature called the knee marks the transition to a steeper decline of flux up to an index of $q \sim 3.3$ until an energy of 10^{18} eV is reached[4]. From there the spectrum hardens considerably again to $q \sim 2,7$. This second key feature first observed by J.Linsley (1963) [38] is traditionally called the ankle and most likely marks the point of the transition from galactic to extra galactic sources.

At energies $2 - 3 \times 10^{19}$ eV a sharp cut-off is observed by the Pierre Auger observatory as well as the HiRes experiment. It remains unclear if this feature is caused by the GZK effect (see Section ???) or a loss in the production mechanism of these particles.

The so called 'Oh-My-God' particle, detected by the Utah Fly's Eye detector marks the end of the spectrum with an energy of 3.2×10^{20} eV.

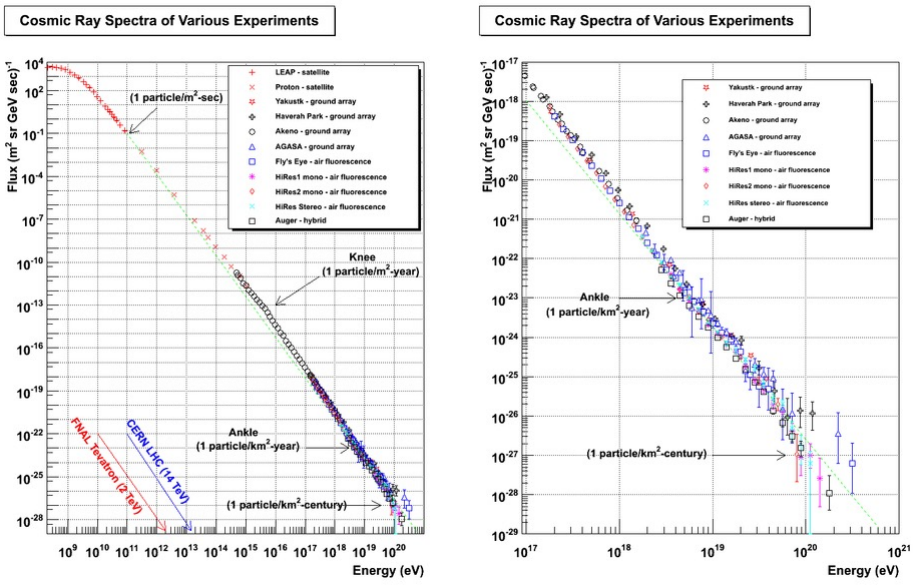


Figure 3 – The particle CR-spectra with the energy range from 10^8 eV to 5×10^{21} eV on the left and from 10^{17} eV to 5×10^{21} eV on the right including the key features knee and ankle. Images: [64]

For particles at energies above the ankle several questions are still unanswered. Neither their origin nor their mass composition is sufficiently understood. Furthermore, the acceleration mechanism is up to speculation and the propagation through the interstellar medium also remains unclear.
The JEM-EUSO program primary objective is to contribute in solving these questions due to the ability of not only gathering higher statistics than any other experiment, but also the precise measurement of the particle energies and their direction[5].

1.1.1 Origin

For energies below the knee, supernova remnants (SNR) are considered as the most likely source of CR, because of their higher magnetic fields compared to the average interstellar medium[32]. Also their shock fronts originated from supernova explosions live long enough to be capable of accelerating particles up to 10^{15} eV. The most common explanation for the particle acceleration through diffusive shock-waves is the Fermi mechanism [31].
Fermi postulated his idea of stochastic particle acceleration in 1949 assuming that charged particles can gain energy through multiple crossing of a shock front, which is moving through interstellar matter. In the original version Fermi described this process in a model where charged particles are reflected by "magnetic mirrors" which are corresponding to perturbances in the galactic magnetic field. These mirrors are assumed to have a random trajectory with a velocity V and if particles stay within the acceleration site for a characteristic time t_{esc} they will gain energy stochastically in these reflections. His calculation showed that the average energy gain per reflection is

$$\left\langle \frac{\Delta E}{E} \right\rangle = \frac{8}{3}\left(\frac{V}{c}\right)^2 \tag{1}$$

if the particles are scattered randomly by magnetic fields. The result shows that the average energy increases only to the second order of the velocity V/c and is therefore called second-order Fermi acceleration. With the assumption of only head on collisions the fractional energy increase is given by $\Delta E/E \propto 2V/c$ and therefore referred to as first-order Fermi acceleration.

With the average time between collisions is given by $\frac{2L}{c}$ with L being the mean free path along a field line, the rate of energy gain is

$$\frac{\mathrm{d}E}{\mathrm{d}t} = \frac{4}{3}\left(\frac{V^2}{cL}\right)E = \alpha E. \tag{2}$$

The diffusion-loss equation describes the resulting spectrum for the time t_{esc}

$$\frac{\mathrm{d}N}{\mathrm{d}t} = D\nabla^2 N + \frac{\delta}{\delta E}[b(E)N(E)] - \frac{N}{t_{esc}} + Q(E). \tag{3}$$

For the steady state solution with no diffusion ($\mathrm{d}E\mathrm{d}t = 0$) an no sources ($Q(E) = 0$), the term $b[E)$ no is the energy gain term $b(E) = -\alpha E$ and this equation gets reduced to

$$-\frac{\mathrm{d}}{\mathrm{d}E}[\alpha E N(E)] - \frac{N(E)}{t_{esc}} = 0. \tag{4}$$

After differentiation the is equation is

$$\frac{\mathrm{d}N(E)}{\mathrm{d}E} = -\left(1 + \frac{1}{\alpha t_{esc}}\right)\frac{N(E)}{E} \tag{5}$$

and therefore

$$N(E) = constant \times E^{-x}, \tag{6}$$

with $x = 1 + (\alpha t_{esc})^{-1}$, which results in a power-law for the energy spectrum and fits the observed CR spectrum[6].
The Fermi mechanism can also be formulated in an alternative way. First two constants are defined, whereas P is the probability of the particle staying in the acceleration site and β which describes the factor of the energy gain after one collision ($E = \beta E_0$). After k reflections $N = N_0 P^k$ particles with energies $E = E_0 \beta^k$ remain. With

$$\frac{\ln(N/N_0)}{\ln(E/E_0)} = \frac{\ln P}{\ln \beta} \tag{7}$$

k can be removed and the equation can be rearranged to

$$\frac{N}{N_0} = \left(\frac{E}{E_0}\right)^{\ln P/\ln \beta}. \tag{8}$$

Here N can be substituted by $N(E)$ since it gives the number of particles reaching E, so

$$N(E)\mathrm{d}E = constant \times E^{-1+(\ln P/\ln \beta)}\mathrm{d}E \tag{9}$$

which is also a power-law for the energy distribution.

Derived from Fermis considerations the diffusive shock acceleration model was developed by several groups independently in the late 70s. The papers from Axford et al. (1977)[33], Krymsky (1977) [34], Bell (1978) [35] and Blandfort and Ostriker (1978) [36] describe this model as first-order Fermi acceleration in presence of strong shock fronts.
in his paper Bell gave the fractional energy increase with

$$\left\langle \frac{\Delta E}{E} \right\rangle = \frac{4}{3}\left(\frac{V}{c}\right) \tag{10}$$

and determined the constants β and P quantitatively for the complete acceleration process with

$$\frac{\ln P}{\ln \beta} = -1. \tag{11}$$

With these constants inserted into equation 10, the differential energy spectrum is

$$N(E)\mathrm{d}E = constant \times E^{-2}\mathrm{d}E. \tag{12}$$

The spectral index of q 2 differs from the measured q $2.5 - 3$, but this result provided a good reason why a power law energy spectrum with a distinctive spectral index is expected for particles accelerated by strong shock fronts.
Lagage and Cesarsky (1983) [37] gave an in depth review of the processes limiting the acceleration and calculated an upper energy limit of $E_{max} = 10^{14}\,\mathrm{eV}$. So particles with energies above $10^{15}\,\mathrm{eV}$ are highly unlikely produced by SNRs.

For UHECRs two models have been proposed:
The bottom-up model explains the steepening of the spectrum above the knee with an intrinsic limit of the mechanism accelerating the particles. The Larmor-radius (see Section ???) of the accelerated particle, which is proportional to the size and magnetic flux density of the accelerating region, has to be smaller than the region itself in order to prevent the particle from

leaving the accelerator.
Figure ??? shows the few known sources that fulfil this condition for protons up to energies of 10^{20} eV, which are:

- Galaxy cluster shocks
- gamma-ray bursts
- active galactic nuclei jets
- jets from radio galaxies
- neutron star magnetospheres

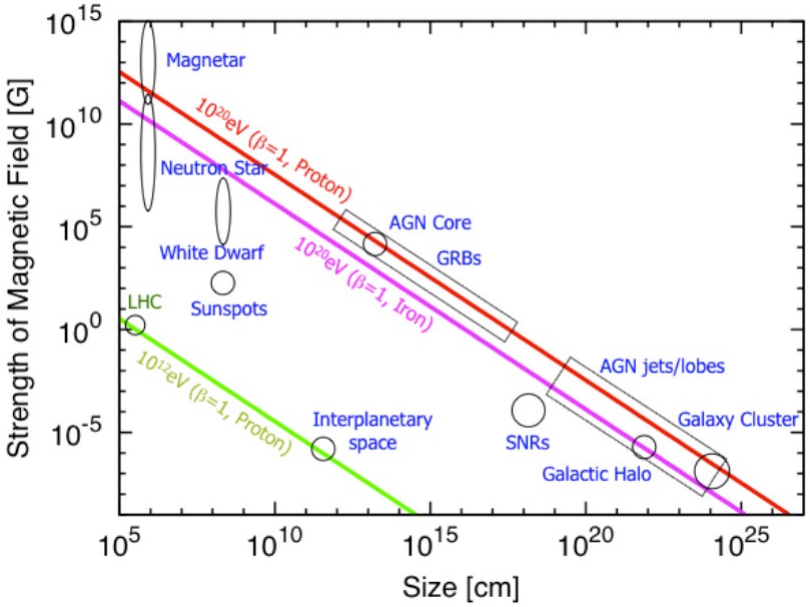


Figure 4 – The Hillas diagram showing the potential candidates for UHECR production. The theoretical upper limit on the energy of particle acceleration with 10^{20} eV is drawn in red, while the upper limit on the energy produced at the LHC (10^{12} eV) is drawn in green for comparison. All the possible sources are very close to 10^{20} eV, proposing a steepening above this energy. If however the flux remains stable above this limit, this would indicate the existence of yet unknown UHECR sources. Image: [65]

The second approach proposed for the origin of UHECR is called the top-down model. It predicts the production of UHECR as a result of decaying or annihilating super-heavy particles (SHP) with a mass between 10^{22} eV and 10^{25} eV. These so called weakly interacting super massive particles (WIMP) are assumed to be produced by the Big Bang, and are also candidates for cold dark matter. They are expected to be distributed isotropically, with an accumulation around galaxies and their halo. According to this theory, the distribution of UHECR should also peak around galaxy halos.
While results of the Pierre Auger Observatory might indicate a correlation of positions of AGNs and observed UHECR[7], a similar study from the HiRes experiment did not show an anisotropic distribution[8]. As the statistics of both experiments are too low to put a conclusion, the JEM-EUSO program might be able to determine which model is more likely in the future.

1.1.2 Propagation from source to the Earth

On their way to Earth, CRs are mainly affected by galactic and extragalactic magnetic fields, changing their trajectory. Furthermore above a certain energy UHECRs start to interact with the cosmic microwave background (CMB). Additionally their flux gets reduced from attenuation, as secondary particles such as photons and neutrinos are produced.

Magnetic fields

As CRs are primarily charged particles, their directions are influenced by magnetic fields. The Larmor-radius r_{Larmor} of the particles with the atomic number Z, which specifies the circular motion of a charged particle in a homogeneous magnetic field B, is proportional to the particles energy E:

$$r_{Larmor} = \frac{E}{ZeB} \tag{13}$$

If this gyro-radius is considerably smaller than the dimension of a galaxy, the galactic magnetic fields wont allow the particle to leave. Considering a uniform magnetic field with $2\,\mu$G and 20 kpc diameter, the threshold energy value would equal $E = 3 \times 10^{19}$ eV.
Particles within and above this value can escape the galaxy and would only be weakly influenced by the magnetic field.
This consideration leads to the assumption that UHECRs have a predominantly extragalactic origin. However it is very difficult to estimate this energy threshold correctly, because the strength of the galactic magnetic field is hard to measure, due to our position within the galaxy [39], and not homogeneous [40].
Additionally the Intergalactic magnetic field, the magnetic field of the heliosphere and the magnetic field of the galactic halo can influence the trajectories of CR, but the strength of the effect is also difficult to gauge, as their strength and distribution are are largely unknown as well [41].

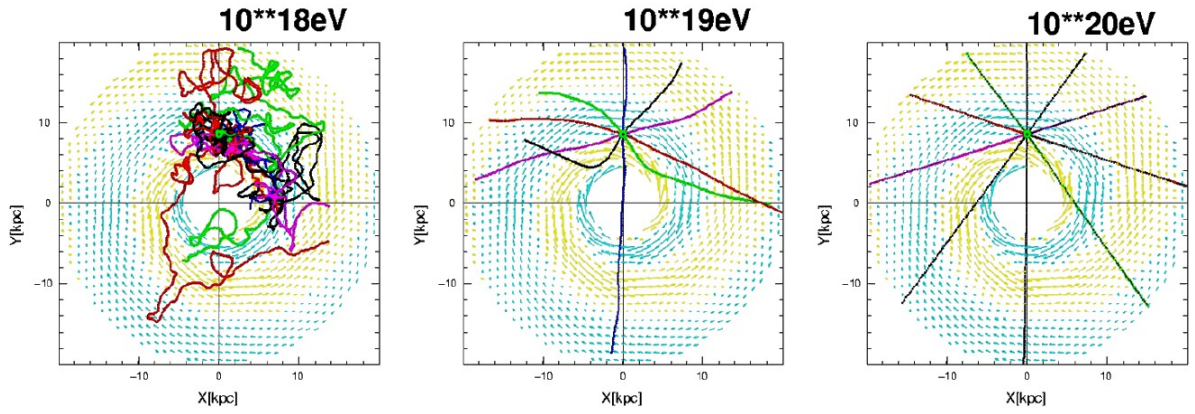


Figure 5 – The simulated propagation of a proton within a galactic magnetic field. The left figure shows that CRs with an energy below 10^{18} eV are trapped within the galaxy. The second figure shows that particles with energies of 10^{19} eV are able to escape the galaxy, though they are still deflected. The right figure shows that the tracks of particles with energies of 10^{20} eV are nearly unaffected by galactic magnetic fields. Image: [66]

The GZK-effect

Greisen (1966) [42] and simultaneously Zatsepin and Kuz'min (1966) [43] proposed that protons with energies above the threshold of 5×10^{19} eV will interact with photons from the CMB, which

is called the GZK-effect. As the UHECRs have very large Lorentz factors, CMB-photons have high energies in the CRs restframe leading to photo-pion and photo-pair production.
Three reactions are possible:

$$\gamma + p \rightarrow n + \pi^+ \tag{14}$$

$$\gamma + p \rightarrow p + \pi^0 \rightarrow p + \gamma + \gamma \tag{15}$$

$$\gamma + p \rightarrow p + N\pi \tag{16}$$

With an average energy of the CMB-photons of $\epsilon_0 = 6 \times 10^{-4}\,\mathrm{eV}$ the photon energy in the rest frame of the CR is

$$\epsilon = \epsilon_0 \gamma \left(1 + \frac{v}{c} cos\theta\right). \tag{17}$$

With the limits $cos\theta = 1$ and $v \rightarrow c$ the resulting energy threshold for the proton is $E = 2\gamma m_p c^2 = 1,7 \times 10^{20}\,\mathrm{eV}$. This value gets lowered to $E = 5 \times 10^{19}\,\mathrm{eV}$ if we consider that a proper calculation would include the integration over the Planck spectrum of the CMB-photons in all directions. With a reactions cross-section of 250 microbarns and a photon count of $N_{photon} = 5 \times 10^8\,\mathrm{m}^{-3}$ the free path length for a single scattering process is $\lambda = (\sigma_{\pi p} N_{photon})^{-1} = 10^{23}\,\mathrm{m}$. With an energy loss of about 10% per interaction protons with energies above the GZK cut-off cannot be originated from further than 30 Mpc from our galaxy. Since the cut-off energy depends on the Lorentz factor γ, the threshold energy will vary for particles other than protons[6].

Pair production

Ultra high energy gamma rays (UHE-γ) can be affected by pair production

$$\gamma_{UHE} + \gamma \rightarrow e^+ + e^- \tag{18}$$

and inverse Compton scattering

$$e^\pm + \gamma \rightarrow e^\pm + \gamma. \tag{19}$$

Photon Pair production results in an effective energy loss on length scales of the order of 10 Mpc and will shift UHE-γ energies down to GeV region [44], whilst inverse Compton mechanism can lead to an increase in flux in the TeV energy range [45]. Additionally, pair production by protons(PPP) can also occur:

$$p^+ + \gamma_{CMB} \rightarrow p^+ + e^+ + e^-. \tag{20}$$

This mechanism has been proposed to be responsible for the dip feature between $E = 10^{18}\,\mathrm{eV}$ and $E = 5 \times 10^{19}\,\mathrm{eV}$ just before the GZK cut-off[9].

1.1.3 Observation Principle and Requirements

For CRs with energies below $E = 10^{15}\,\mathrm{eV}$, the flux is large enough for experiments that directly collect events in detectors from a balloon or space using simple scintillation counters. When a CR hits the scintillator it generates photons that can by measured by photo-multipliers. This method though is unfeasible for UHECRs due to much smaller flux, making a direct measurement impossible. UHECRs impinging the atmosphere however start to interact with air nuclei resulting in extensive air showers (EAS), whose secondary particles can be observed. In the first stage, the UHECR generates many hadrons, which either decay in muons, electrons and photons, or also interact with other nuclei resulting in more hadrons until the energy threshold for these interactions is reached. The resulting photons have still enough energy for

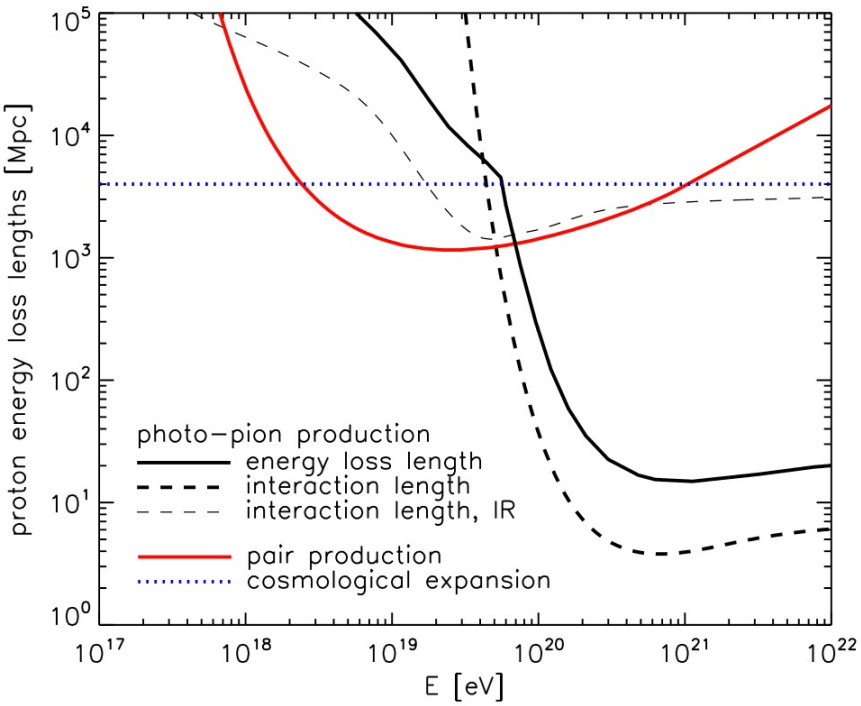


Figure 6 – The figure describes the energy loss of UHECRs due to the GZK-effect (black lines), the pair production (red line) and the cosmological expansion (blue pointed line). Image: [46].

pair production and a part of the produced electrons ionize nitrogen, again producing photons in the UV-range between $E = 330\,\text{nm}$ and $E = 400\,\text{nm}$ called flourescence light. Primary particles with higher energies have the capability to produce more electrons and therefore the amount of UV-photons correlates proportionally to the UHECR energy.
Additionally, Cherenkov photons are produced by the secondary particles propagating faster than the speed of light through the atmosphere. While ground based experiments either focus on muon detection as the Pierre Auger Observatory, or detect the Cherenkov light as the HESS telescope, the JEM-EUSO approach is to observe the flourescence light. The reason for it is the isotropic radiation trajectory from the shower axis which allows a derivation of the CR direction as shown in Figure ???.
An event seen with JEM-EUSO will appear as a luminous spot covering several pixels and moving in a direct trajectory at nearly the speed of light. This is shown in Figure ??? for one Photo-Detector Module (PDM) and the whole instrument. By measuring the amount, the light profile and the trajectory of the UV-photons, the JEM-EUSO telescope can reconstruct the energy, direction and type of the event, which is discussed in detail by Mernik(2009)[10].

Requirements

The JEM-EUSO consortium defined a list of requirements necessary for a successful mission (JEM-EUSO collaboration, 2010)[2]. The Observation requirements are derived from the science objectives while they also define the required performance of the instrument.

Science requirements:

SR1: Specification of UHECR origin by arrival direction analysis with determination accuracy better than a few degrees

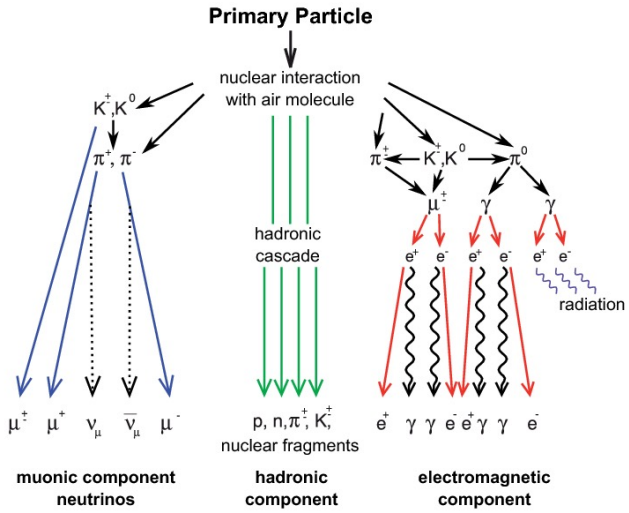


Figure 7 – Schematical drawing of EAS with flourescence light (purple) and Cherenkov light (blue). Image: [67]

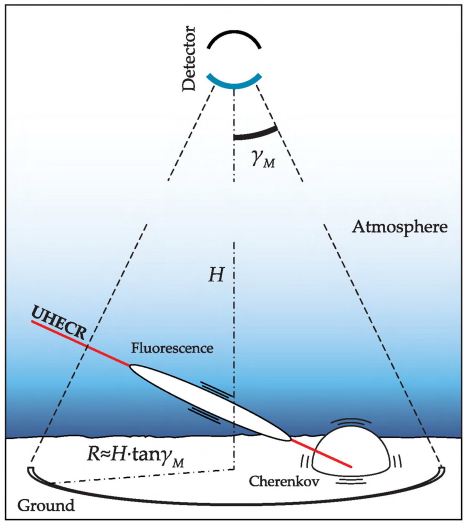


Figure 8 – Concept of UHECR detection via fluorescence light from space. Image: [63]

SR2: Determination of trans-GZK structure in cosmic ray energy spectrum

SR3: EECR primary identification capability: discriminating among nucleus, gamma ray and neutrino

SR4: Observation capability of TLEs

Observation requirements:

OR1: Observation area: $\geq 1.3 \times 10^5 \left(\frac{H_{orbit}}{400\,\mathrm{km}}\right)^2$ km^2 [SR1]

OR2: Arrival detection determination accuracy: $\leq 2.5°$ ($E = 10^{20}$ eV and 60° zenith angle) [SR2]

OR3: Energy determination accuracy: $\leq 30\%$ ($E = 10^{20}$ eV and 60° zenith angle) [SR3]

OR4: X_{max} determination accuracy: $\leq 120\,\frac{\mathrm{g}}{\mathrm{cm}^2}$ ($E = 10^{20}$ eV and 60° zenith angle) [SR4]

OR5: Energy threshold: $\leq 5.5 \times 10^{19}$ eV [SR1]

OR6: Monitoring the average signal rate for all pixels every 3.5 s [SR4]

OR7: Capability of observing TLE with time scales shorter than 1 s [SR4]

Instrument requirements:

IR1: Observation duty cycle: $\geq 17\%$ [SR1]

IR2: Instrumental duty cycle: $\geq 30\%$ [SR1]

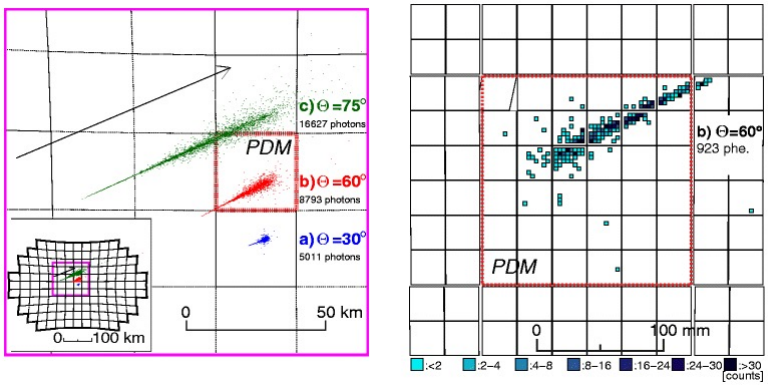


Figure 9 – The left figure shows the projected tracks for three EAS with energies of $E = 10^{20}\,\mathrm{eV}$ and zenith angles of a: $\Omega = 30°$, b: $\Omega = 60°$ and c: $\Omega = 75°$. The dot density represents the amount of photons detected by JEM-EUSO. The right figure shows the b case for a single PDM, which would be the case for EUSO-SPB. Images courtesy of the JEM-EUSO collaboration [47].

IR3: Lifetime: longer than 3 years. Two-year storage is also required for launch [SR1]

IR4: Attitude determination accuracy: $\leq 0.05°$ (this may be achieved by offline analysis) [OR2, OR3, OR4]

IR5: Precision of absolute time: $\leq 1\,\mu\mathrm{s}$ [OR2]

IR6: Wavelength band: covering major fluorescence lines in 330 nm to 400 nm [OR1, OR2, OR3, OR5]

IR7: Synchronization precision among subsystems: $\leq 200\,\mathrm{ns}$

IR8: Light shield against stray light: less than GHz level [OR2, OR5]

1.2 Additional Objectives

Besides the main objective of observing UHECRs, the UV telescope with its high time resolution in addition with the IR-system and lidar onboard can also observe meteors, meteoroids, TLEs and other atmospheric phenomena.

Extreme energy gamma rays

The airshowers induced by gamma rays differ significantly from UHECR induced EAS making both types distinguishable. The Landau, Pomeranchuk and Midgal effect (LPM) [48] [49] [50] shrinks the cross-section of bremsstrahlung and pair production considerably for photons with energies above $5 \times 10^{19}\,\mathrm{eV}$ leading to a later first interaction, which results in a smaller shower profile at sea level. Besides gamma rays have the ability to interact with the magnetic field of the Earth in an altitude of 1000 km producing positron-electron pairs. This leads to a shower maximum in much higher altitudes than for UHECRs.

Extreme energy neutrinos

High energy neutrinos are also able to produce EAS as their cross-section enlarges with their energy. Due to their very small cross-section for interaction with nuclei, neutrino EAS are occurring either deep in the atmosphere or directed upwards, making them also discriminable from UHECR events. The emerging Cherenkov light might be detected by JEM-EUSO. A thesis about their detection rate and angular reconstruction by JEM-EUSO was written by Bittermann (2010)[11].

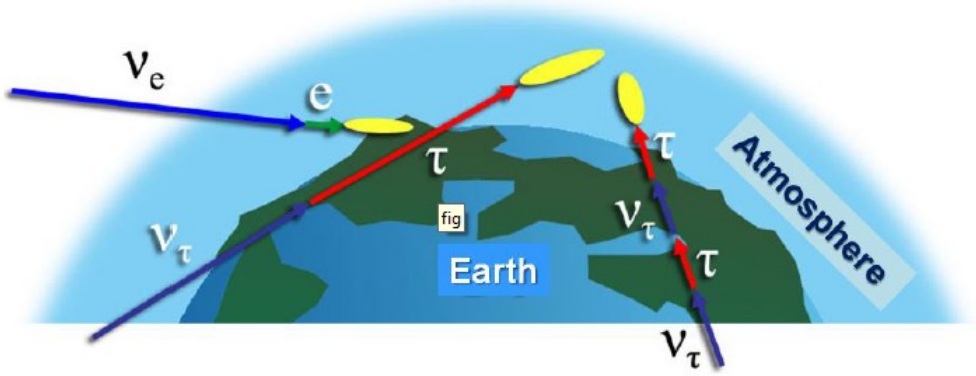


Figure 10 – Schematic view of extreme energy neutrino EAS. Neutrinos at energies $\geq 10^{20}$ eV can produce airshowers near to the earth's surface. Tau neutrinos also may induce upwards EAS after passing through the earth, while Electron and muon neutrinos are absorbed by the earth. Image: [2]

The galactic magnetic field (GMF)

If JEM-EUSO is able to identify a point source from events above 10^{20} eV, events with lower energies can also be detected from this source. The differences in arrival direction, magnitude and energy of those events will enable to determine the GMF. With their Larmor radius being much larger than the GMF, the particles are deflected adiabatically and are not spread away from the source. The shape of the events however is deformed by a few degrees along the line of sight, depending on the strength of the GMF, which allows a rough estimate about its structure and intensity[51].

Meteors

When meteors arrive at the Earth, their kinetic energy is converted into heat via friction with the surrounding air molecules. The temperatures can reach 2500 K, which is enough to ionize the surrounding matter along the trajectory. The resulting ions and free electrons produce a photon-spectrum from the IR to the UV range. The spectrum contains black-body radiation as well as nitrogen and oxygen lines. The surveillance of meteors is a major concern of current planetary science, as they can pose a major threat to nature and human life on Earth.
In comparison to ground based meteor observatories the JEM-EUSO telescope with its high sensitivity in the UV range can provide coverage of a wider area with a higher duty cycle as it is less dependant on weather conditions.

Transient luminous events (TLE)

First observed in 1989 [12] TLE is an umbrella term for various light flashes on top of clouds. The phenomena are classified in the following way:

- **Sprites** are light flashes occurring in an altitude between 40 km and 90 km above thunderstorms. As they last only a few ms, observation with time resolution within the order μs will help to understand their origin.
- **Halos** are luminous discs in an altitude between 70 km and 85 km which might precede sprites but also occur alone.
- **Elves** are toroid shaped emissions in the ionosphere ($\sim$ 90 km) caused by electromagnetic pulses (EMP) from lightning strokes.
- **Blue jets** are jets emitted by an upward electrical discharge from thunderstorm clouds. Their total energy can reach up to 30 MJ.
- **Terrestrial gamma ray flashes (TGF)** are most likely produced by strong electric fields within thunderstorms and were first detected in 1994 by the BATSE of the Compton Gamma Ray Observatory.

JEM-EUSO would help to advance our understanding of TLEs as their emitted spectrum also reaches into the UV range.

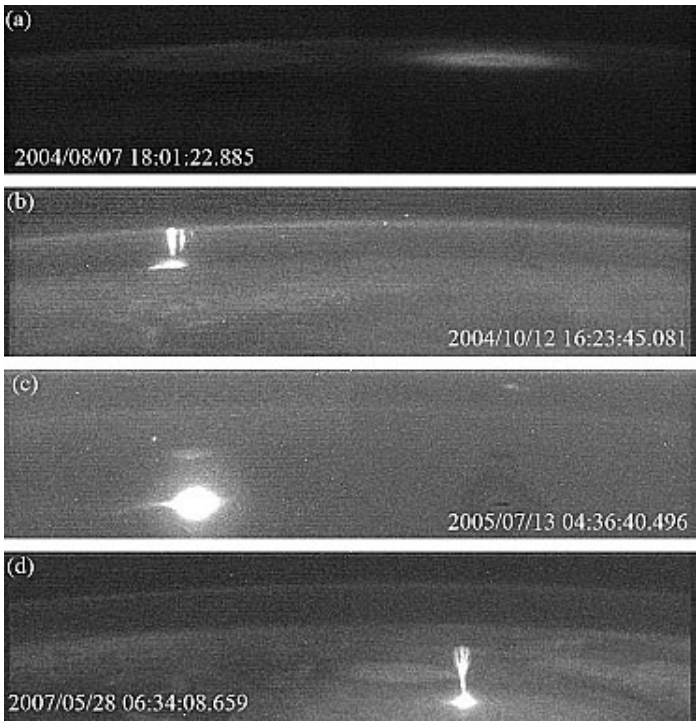


Figure 11 – Different observed TLE-images: (a) elf, (b) sprite, (c) halo, (d) blue jet. Image: [52]

2 The JEM-EUSO Program

2.1 Overview

Originally selected by the European Space Agency (ESA), the first EUSO Observatory was planned to be installed onto the European Columbus module of the International Space Station. After the successful phase-A study in 2004 financial problems led to a stop of the development

until the mission was redesigned as JEM-EUSO by the Japanese and U.S. teams under the leadership of Yoshiyuki Takahashi [13]. The launch was targeted for 2013, but was postponed to 2017 after the phase-A/B1 study which improved the mission profile significantly. As for now, the current mission status does not foresee a launch in the near future
In the framework of the EUSO project several individual missions emerged, using the parts of the telescope developed for JEM-EUSO for calibration, performance testing, and improving the knowledge of the detectors.

2.2 The EUSO-TA Mission

The EUSO-TA mission is a ground based experiment located at the Telescope Array site in Utah, USA. Using the original EUSO PDM with a specially developed optical system consisting of two square Fresnel lenses with a length of 1 m and a FOV of ±6 degrees.
It started operating in February 2015, observing UV-light in the atmosphere and is triggered externally by the TA Black Rock Mesa florescence detectors.
The main mission goal is the calibration of the prototype telescope with the help of two TA laser facilities and their florescence detector. Furthermore, a cross-calibration with the Auger system is planed for the future. Five observation campaigns were performed for a total duration of 48 observation nights between February and December 2015[14].

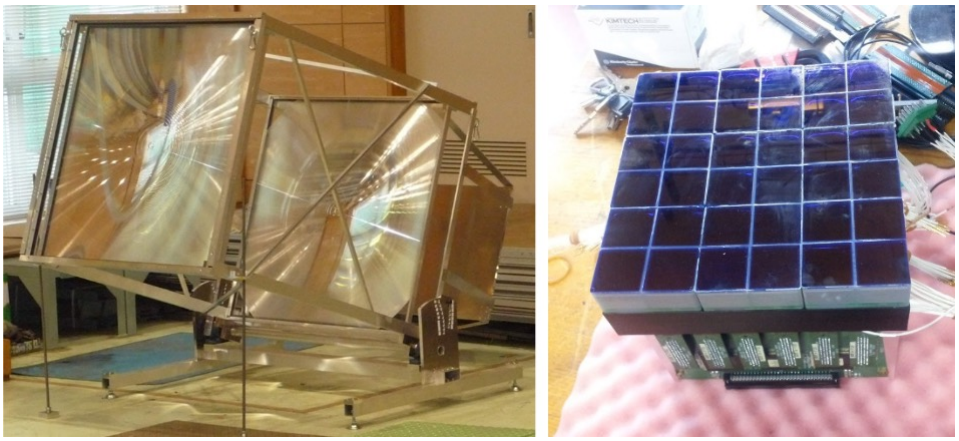


Figure 12 – Left: The EUSO-TA telescope, right: the PDM. Image: [63]

2.3 The Mini-EUSO Mission

The Mini-EUSO mission will be attached to the Zvezda Russian module of the ISS, observing UV-light of the Earth's atmosphere in the nadir position through a UV-transparent window. With two Fresnel lenses and a single PDM, Mini-EUSO is meant to be a precursor for future UV-range missions on the ISS. The compact telescope with a FOV of ±19 degrees and a 2.5 μs time resolution, will be the first to observe UV-light from space with Fresnel lenses.
Its science objectives are mainly studies of atmospheric phenomena described in chapter[?????], but it could also become a pathfinder mission for potential debris removal via laser ablation[15]. The mission is approved by the Russian Space Agency and the Italian Space Agency and the launch is planned for 2017.

2.4 The K-EUSO Mission

Similar to Mini-EUSO the K-EUSO is also a mission approved by the Russian Space Agency Roscosmos and also part of the Russian "Stage program of scientific and applied research and

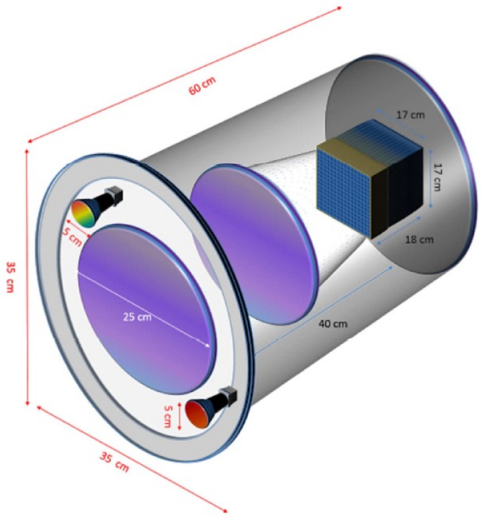


Figure 13 – The Mini-EUSO instrument. Image: [63]

experiments". Compared to the other missions a different optical system based on a Schmidt optics is used. With a pupil diameter of 2.5 m and a spherical mirror of 4 m width, the Schmidt camera is able to achieve a FOV of ±20 degrees. Additionally, an Infra-red camera and a Lidar will be installed for cloud monitoring.
Thanks to the orbit of the International Space Station the telescope is able to observe the whole UHECR sky and find possible hotspots as well as compare UHECR fluxes for both hemispheres. The side objectives are the same as for the JEM-EUSO mission. The mission launch is planned for 2022 with a two year operation time.

2.5 The EUSO-BALLOON Mission

EUSO-Balloon was developed as a pathfinder mission for the JEM-EUSO project in order to test the function and performance of all JEM-EUSO instruments and their subsystems for further missions. The telescope consists of an optical system adapted for the flight altitude of 40 km and one PDM pointing to the Earth from above.
Proposed to the French Space Agency in 2011, the phase-A study was completed in the same year. The phase-B study focussing on the instrument definition end in 2012 and led to the manufacturing by the end of 2013. On August 25th, 2014 the EUSO-ballon accomplished a successful flight for over 5 hours from the stratospheric base in Timmins, Ontario. A helicopter following the balloon shot a UV-laser into the FOV of the telescope to simulate EAS as the flight duration made it unlikely to record any real events.
The telescope recorded 33×10^6 frames and stored them onto the onboard RAID disks. After landing into a small lake the instrument was recovered without significant water damage. The following data analysis showed that the instrument detected the simulated EAS mimicked by laser shots correctly and therefore partly proved the capability of detecting EAS as well as the function of the whole system[1].
In order to prove that the system is able to detect real EAS events as well, the collaboration decided to perform a second Balloon experiment with a much longer flight duration in order to increase the chances of detecting several EAS, called EUSO super pressure balloon (EUSO-SPB).

Figure 14 – Left: The EUSO-Balloon launch at Timmins Stratospheric Balloon Base. Right: The instrument floating in "Lake EUSO". Images: [1]

2.6 The EUSO-SPB Mission

The EUSO super pressure balloon mission will be the first to detect EAS from above the atmosphere. It carries an updated version of the instrument used for the EUSO-Balloon mission and is planned as a long duration flight with a minimum of 30 nights of exposure in order to enhance the exposure for EAS events.
The instrument consists of a $1 \times 1\,\mathrm{m}^2$ UV telescope which has a 12×12 degree FOV and a single PDM with 2304 pixels each with a 0.25×0.25 degree FOV. The UV filter on the PDM is permeable for the UV florescence spectrum from 290 nm to 430 nm. The upgrades to the previous balloon instrument are:

- Higher quantum efficiency multi-anode photomultplier tubes (MAPMTs) (Hamamatsu model R11265-113-M65 MOD2)
- Solar panels and an updated power system with the panels being mounted on the four sides of the gondola, to ensure power stability
- inclusion of the third Fresnel lens according to the original design for chromatic correction
- Updated high voltage distribution system
- Fully implemented level 1 trigger on the PDM
- Updated system control for a 50 day mission
- Interface to the Columbia Scientific Balloon Facility‘s Support Instrument Package (SIP)

The data telemetry transfer is established by two Tracking and Data Relay Satellite System (TDRSS) data links, with a rate of $180\,\frac{\mathrm{kb}}{\mathrm{s}}$. With an expected average trigger event rate of 0.25 Hz and a maximum exposure time of 9 h for very dark nights, the collected data can be downloaded within 24 h. A separate Irridium satellite link is used for sending basic control commands to the instrument control computer.
I was originally planned to also use an aircraft equipped with a UV LED and a pulsed $355,\mathrm{nm}$ laser (16 second pulse duration) to fly below the balloon for the first hours and provides a set of calibration flashes and tracks for the instrument[17], but due to the several delays of the start the onboard LED overtook this task.

After several attempts in March and April 2017 the mission launch, shown in Figure ???, took place in April 24th from Wanaka, New Zealand. Unfortunately likely caused by a leak, which was was not detected at the launch, the balloon lost altitude ongoing from the first night. This forced the surveillance team to discharge ballast every night. At May 7th the operating altitude could not be maintained and the balloon landed on the south Pacific ocean. The flight track is shown in Figure ???. Almost half of the observation data was received via the TDRSS data links and the data analysis is in progress.

Figure 15 – The EUSO-SPB launch from Wanaka at April 24th 2017. Image: [68]

Figure 16 – The EUSO-SPB flight track from Wanaka, New Zealand to the south east Pacific. The original flight plan foresaw a landing in South America after one orbit around the Earth. Image: [68]

3 The JEM-EUSO instruments

3.1 The main instrument

As mentioned in Chapter[???] the first EUSO telescope completed its phase-A study successfully in 2004, before the mission was redefined as JEM-EUSO in 2006. Therefore, the JEM-EUSO 1100 kg refractor telescope is an upgraded version of the ESA-EUSO instrument, which brings several advantages over the original design. The main goal was to reduce the threshold energy while increasing the effective area covered. The technical details will be described in the following sections and are based on the Report on the Phase A Study (The purple book)[2].

The telescope consists of a digital camera, an atmosphere monitoring system and a calibration system. The main features of the camera are a large aperture with a large FOV (±30 degrees), high time resolution (2.5 μs, and high pixel count(0.3 million) with the capability to detect single photons, operating in the UV-range from 330 nm to 400 nm and enabling a spatial resolution of 0.1 degrees.
The main components are the optical subsystem, the focal surface detector, the read out electronics and the mechanical structure.

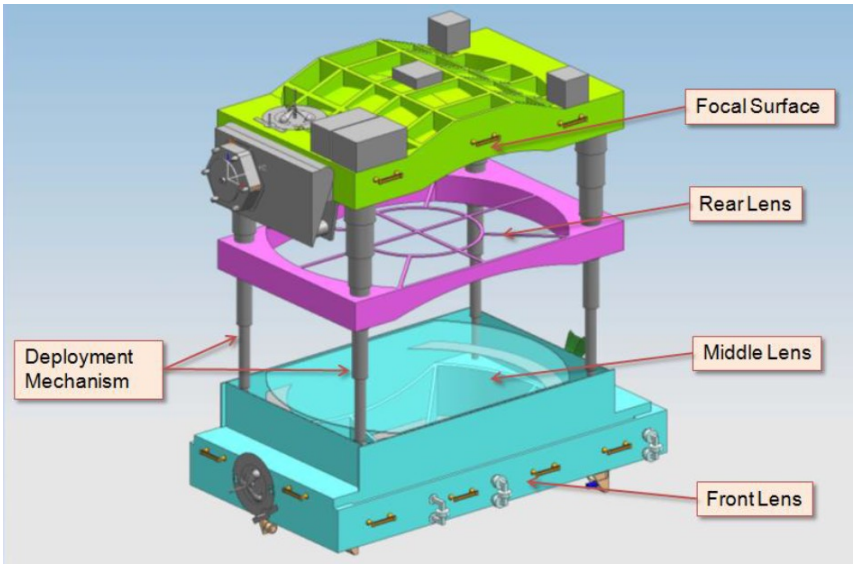


Figure 17 – The mechanical structure of the JEM-EUSO telescope showing the three lenses, the focal surface and the deployment mechanism. Images: [2]

3.1.1 Optical subsystem

Overview

The JEM-EUSO Optics Module (OM) is based on the phase-A design from 2004. The study proposed a refractive system consisting of two curved double-sided Fresnel lenses in PolyMethylMethAcrylate (PMMA). Since then the usage of better performing materials and the introduction of a third intermediate lens compensating chromatic aberration, led to two updated OM versions.
The so called "baseline" optics uses a new PMMA material with better performance called PMMA-000 in the UV-range. The "advanced" option introduces a design in which Amorphous Peffluoro Alkenylvinylether (CYTOP) is used for the front lense, while the other two remain PMMA and is therefore called CPP. CYTOP shows better performance than PMMA but is heavier and has never been tested in space before.

Optical design

The main requirements for the OM are:

- A large diameter for the lenses to increase the photon count collected and therefore to lower the threshold energy for UHECR events.
- a large FOV to cover a wider area enabling the detection of as many events as possible

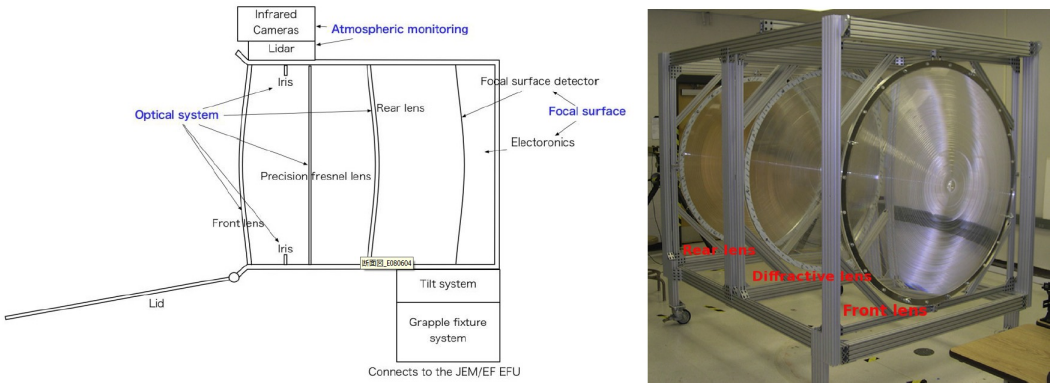


Figure 18 – Left: the conceptual design of the OM. Right: The 1.5 m three lens optics with the focal surface in the rear at the testing site in MSFC. Images: [58]

- the focal number must be as small as possible (f/#$\leq$ 1.25) in order to have a focal surface fulfilling the dimension and weight constraints

For both the baseline and the advanced design the lenses diameter is 2.65 m with a side-cut to 1.9 m necessary due to the dimensional restrictions of the H-II Transfer vehicle (HTV). This configuration also achieves a significant weight reduction, while the performance loss stays negligible up to a 15 degree field angle. The FOV is decreased to $\sim$ 24 degrees by this measure (compare figure ???).
However the possibility of using a Space-X Falcon 9 launcher and Dragon transport vehicle instead of the HTV allows the usage of the circular optics which impacts the instruments performance positively[16].

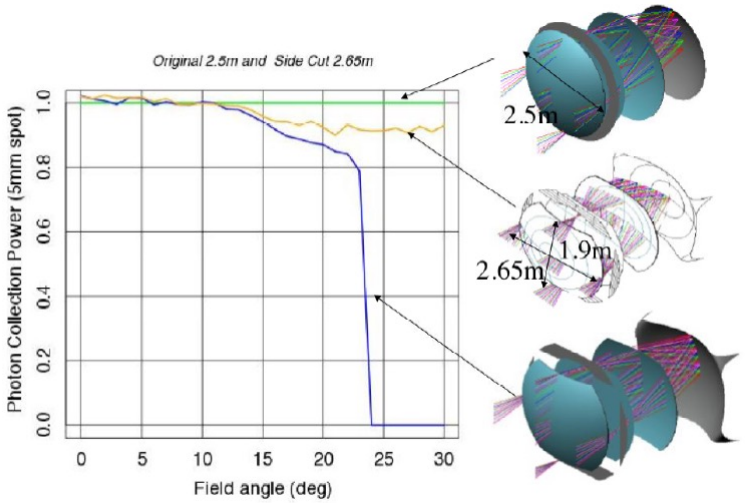


Figure 19 – The performance comparison between the the original design and the side-cut configuration. Yellow line: parallel direction from side-cuts. Blue line: vertical direction from side-cuts. The performance difference is visible from a 15 degree angle and the FOV is decreased to $\sim$ 24 degrees for the side-cut configuration. Image: [2]

In addition to the usage of PMMA instead of CYTOP for the first lens, the baseline design allows a further weight reduction as the outer parts of the first lens are unused (compare Figure ???). This results in a mass difference of 48 kg which is compensated by the better performance of the advanced design. Table ??? compares the main properties with respect to

the requirements of both designs, while Figure ??? shows the spot sizes for different incident angles.

Table 1 – Comparison of both designs with the mission requirements. Table: [22]

	Requirement	Baseline	Advanced
f/# (F number)	< 1.25	1.0	1.0
Lens diameter	≥ 2.5 m	(2.3 m) 2.65 m	2.65 m
Spot size (RMS)	≤ 5 mm	≤ 2.2 mm	≤ 1.6 mm
Throughput	50%@0°-10° 40%@10°-20° 30%@20°-30°	59%@0°-10° 52%@10°-20° 39%@20°-30°	62%@0°-10° 58%@10°-20° 42%@20°-30°
Mass	≤264 kg	154 kg	202 kg

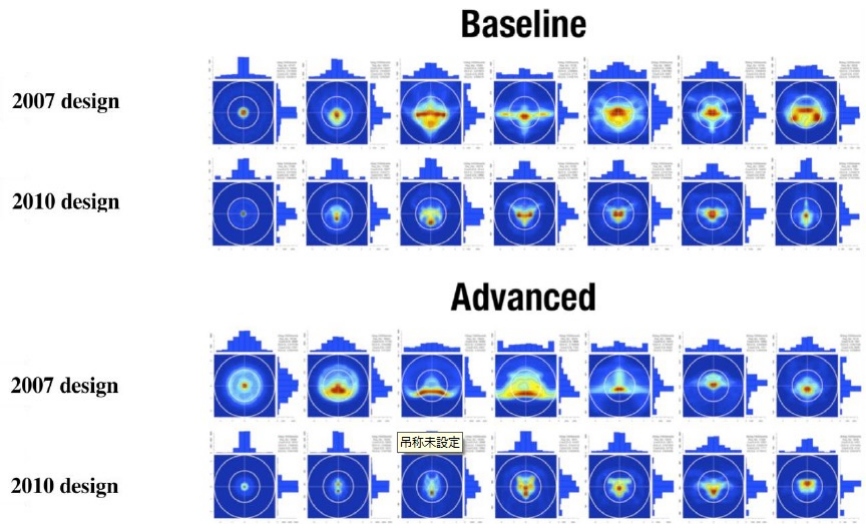


Figure 20 – Comparison of the spot sizes for both designs. The incindent angles are from 0 to 30 degrees in 5 degree steps from left to right. The white circle diameters are 2.5 mm and 5 mm. Image: [2]

The OM itself consists of:

- The first (nadir) lens. which is a curved doublet Fresnel lens.
- The iris which decreases stray light and the entrance pupil diameter.
- The second lens, which has a Frensel surface on one side and a diffractive surface on the other side.
  The Fresnel surface serves as field lens reducing the spot size from 5 mm to 2.5 mm.
  The diffractive surface reduces the chromatic aberration induced by the variation of the PMMA refractive index for different wavelengths.
- The third lens, which is again a curved doublet Fresnel lens focusses the incoming photons on the focal surface.
- The UV-filters at the surface of the MAPMTs, the lens frame and the focus-adjust-system

Based from the design concepts presented above three different models have been realized. A 1.5 m optical system with circular lenses has been build and tested at the Marshall Space flight Center (MSFC), with test results surpassing the requirements. For the EUSO-TA mission

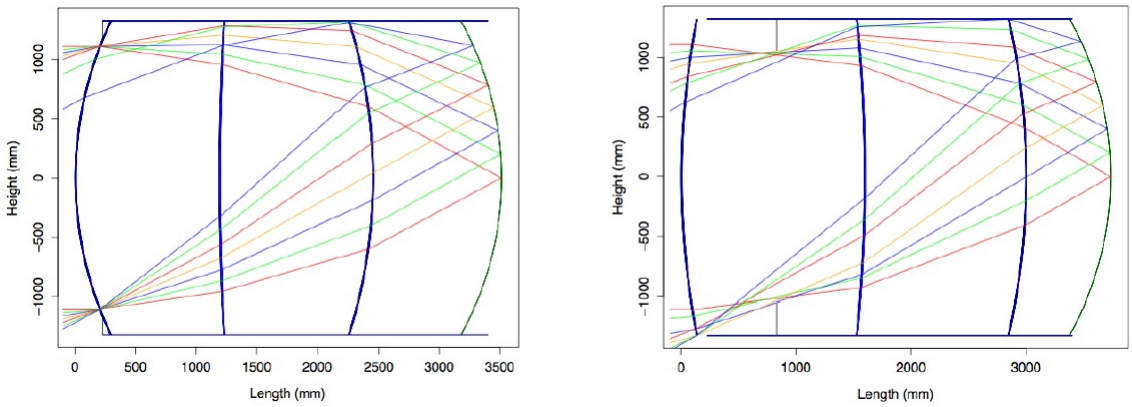


Figure 21 – The cross-section views for both designs. Image: [2]

a two lens system with a 1 m diameter was build and installed at the Telescope Array in Utah. For the EUSO-Balloon pathfinder mission as well as the EUSO-SPB mission a three lens system with a quadratic $1 * 1\,\mathrm{m}^2$ setup was used for the flights in August 2014 and April to ??? 2017.

3.1.2 Focal Surface

The Focal Surface (FS) is placed in the focal spot of the telescope and has a spheric curvature with a diameter of 2505 mm. It is covered with 4932 Multi-Anode Photon Multiplies (MAPMTs) with 64 pixels each which corresponds to a total pixel count of 315648 with a spatial resolution of 0.074 degrees for each pixel. Each MAPMT is controlled by one Application-Specific Integrated Circuit (ASIC) and converts photons to electrical pulses with 2 ns width, which fulfils the response performance requirement. The ASIC accumulates the pulses during one Gate Time Unit (GTU) of 2.5 μs. A 2×2 array of MAPMTs forms one Elementary Cell (EC), while a set of 3×3 ECs are integrated in one PDM.

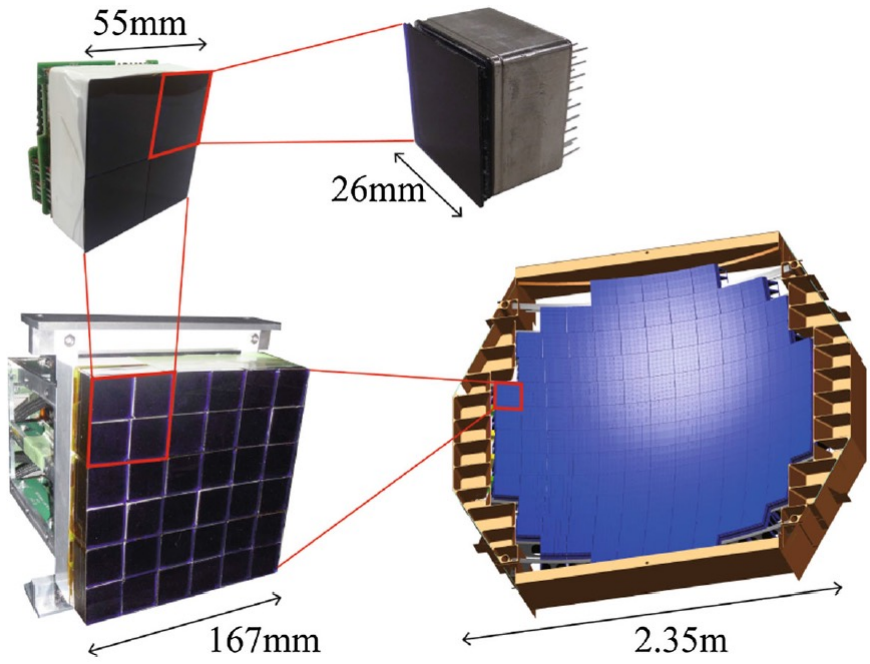


Figure 22 – Composition of the FS. Four MAPMTs (top right) form a EC (top left). The PDM (bottom left) consists of nine ECs or 36 MAPMTs, while 137 PDMs cover the FS (bottom right). Image: [58]

The JEM-EUSO Collaboration defined the requirements for the detector in 2010:

Performance requirements:

- The FS shall be capable to detect the EAS by observing the fluorescence light produced during the EAS development and the Cherenkov light.
- The FS shall be capable to determine the position of the arriving photons as a function of time and to follow the space-time development of the EAS.
- The FS shall have single-photon sensitivity in the 330 nm to 400 nm wavelength range to detect EAS as faint as possible.
- The FS shall have fast response (below 0.1 μs) to follow the EAS space-time development.
- The FS pixel size FoV shall not be greater than $\Delta\alpha = 0.1\,^{\circ}$.
- Cross talk between neighbouring pixels shall be less than 10 % (TBC).
- The noise rate shall be two orders smaller than the rate of the night airglow background.
- Overall detection efficiency shall be good and uniform. The overall detection efficiency, averaged over all the FS, shall be $\epsilon^{PD} \geq 0.12$.
- The FS shall cover the optical focal surface with a sensitive area as large as possible by reducing dead or inefficient areas.
- The FS shall have low sensitivity to magnetic fields of the order of magnitude of 1 Gauss.
- The FS shall be highly reliable and stable over at least a five years‘ time.
- The FS shall be compatible with the requirements imposed by a Space Mission.

Physical requirements:

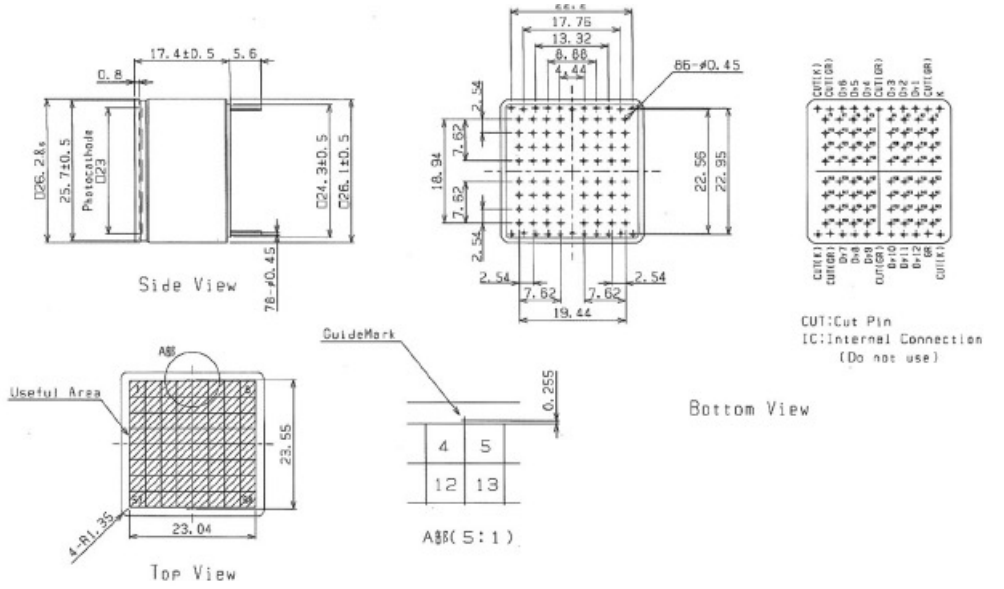
- The mass of optics is defined by the JEM-EUSO Instrument System.
- The FS structure must be totally included in the JEM-EUSO telescope envelope.

Thermal requirements:

- The FS shall be designed so that the temperature does not exceed 50 °C at any time, to protect the bialkali photocathode.
- The FS shall be designed so that the temperature must not fall below −30 °C for the operation safety of the electronics.

3.1.3 The multi-anode Photomultipliers

Developed by RIKEN in collaboration with Hamamatsu Photonics [53], the MAPMT consists of 8×8 pixels with ultra-bialkali photo-cathodes, which reach a quantum efficiency higher than 35 %. Its dimensions are 26.2 mm × 26.2 mm × 20.25 mm with a 2.88 mm pitch and a 1.6 mm dead zone at the borders [54]. The PMT is covered with a 2 mm UV-filter with a trapezoid shape in order to redirect the light at the borders and between the tubes into the PMT. This results in a higher photon count at the border-pixels of the MAPMT, while the distance between the pixels is negligibly small with less than 100 μm. A metal channel dynode structure in the MAPMT provides a photon gain of 10^6 at 0.9 KV with a pulse rise time of $\sim$ 1 ns and a transit time spread of 0.3 ns. The pixel efficiency is 22 % with a pixel dispersion of 30 %, which exceeds the performance requirements for detection efficiency. A Cockroft-Walton (CW) circuit serves as voltage multiplier for the PMT providing 60 V for each stage up to 1.1 KV [53]. In case of strong illumination like for example TLEs the anode voltage must be switched down in order to prevent damage of the PMT, which decreases the photon efficiency while the gain stays the same.



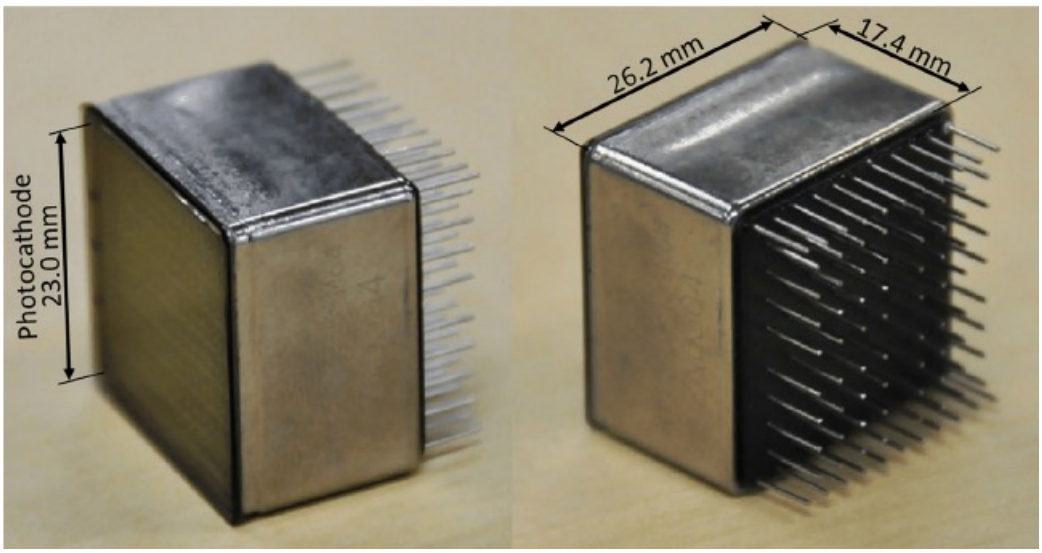


Figure 23 – The Hamamatsu MAPMT unit with its dimensions at the top and side views at the bottom. Image: [58]

The advances made in the development of Silicon photomultipliers (SiPM) in the last years have led to the decision to possibly also implement them instead of the MAPMTs in the near future. SiPMs have several advantages over common PMTs, as better timing resolution and faster response time, but most importantly their supply voltage is between 15 and 75 times lower than for traditional PMTs [55]. This makes the high voltage supplies redundant, which are error-prone and always pose a high risk when implemented in space missions. Additionally since SiPMs diameter is much smaller a significantly higher resolution could be achieved with an updated FS in the future [56].

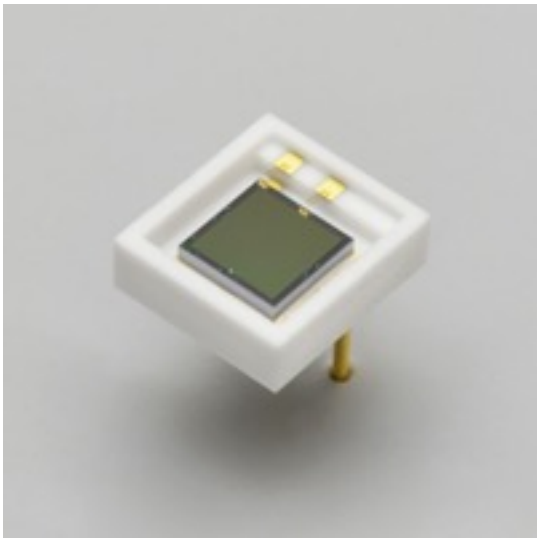


Figure 24 – The Hamamatsu Multi Pixel Photon Counter (MPPC) SiPM currently used at the Tokai to Kamioka (T2K) experiment. Image: [69]

3.1.4 The Focal Surface Electronics

The electronics of the JEM-EUSO telescope consist of the Focal Surface (FS) Electronics and the Control Electronics. While the FS Electronics is directly attached to the focal surface itself the Control Electronics is located in shielded electronic boxes. Its general architecture is shown in Figure ???.

The FS Electronics includes:

- The front end electronics (ASIC SPACIROC) [18] performs reading out and controlling the MAPMTs, analog to digital conversion and counting of the pulses.
- The PDM electronics: responsible for collecting the data of 36 SPACIROCs, performing the Level 1 tripger and sending the data the the Cluster Control Board (CCB).
- The Cluster control board electronics: performs a further data reduction and data management.
- The FS power supply system: provides the low and high voltage power for the whole system.

The Control Electronics includes:

- The ISS (JEM) communication interface: establishes a communication uplink for data read out and control commands with the TDRSS.

- The FS assembly communication interface: handles the link between FS and Control electronics.
- Scientific function management system: responsible for the data acquisition and storage system.
- Housekeeping (HK) collection management system: monitors HK data from all electronic systems.
- several management systems: responsible for LIDAR. IR camera. Thermal Control, the Calibration, Monitoring and Alignment device and the Lid mechanism.

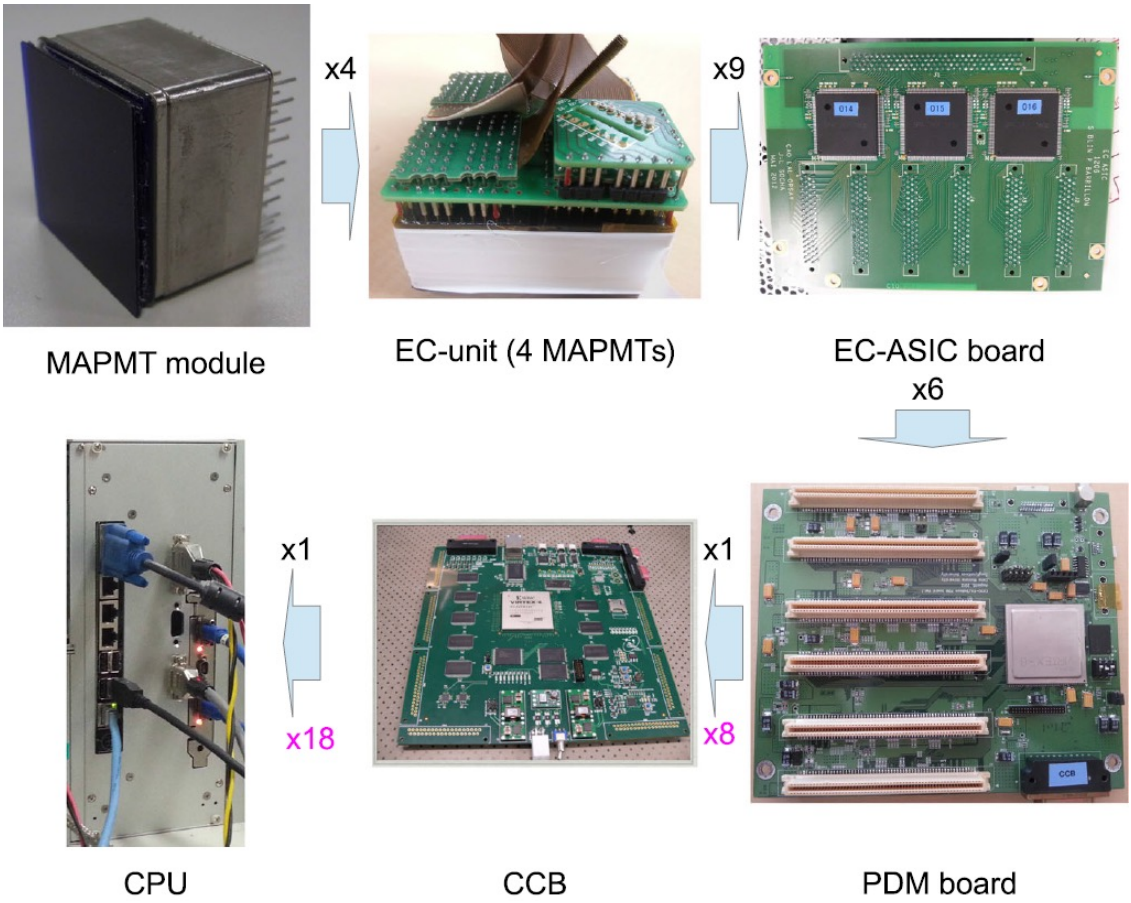


Figure 25 – The signal handling of the FE electronics. The multiplication numbers between the subsystems are black for EUSO-TA, EUSO-Balloon and EUSO-SPB and pink for the full JEM-EUSO mission. Image: [58]

3.1.5 The Front-End Electronics (FEE) - ASIC SPACIROC

The Spatial Photomultiplier Array Counting and Integrating Chip (SPACIROC) performs the read-out operation and control of the MAPMT. It is currently being developed at the Laboratoire de l'Accélérateur Linéaire (LAL) in France and divided into three main units: the Photon Counting (PC) and the Charge to Time (Q-to-T) converter also called KI, which are implemented in the analog part, and the Digital Counters and read-out as well as the slow control registers and the signals monitoring, which lie in the digital part of the chip. The SPACIROC is specifically designed for low power consumption and maximum tolerance against Single Event Latchup (SEL) and Single Event Upset (SEU) effects [18].

Three version have been developed so far: The SPACIROC1 which was used for the EUSO-Balloon mission met all necessary requirements. The second version improved power consumption and overall performance. The latest version SPACIROC3 was designed with a new front end in order to improve the double pulse separation and charge dynamic range and has been used to equip the current EUSO-SPB mission[19].
After the original plans to assemble the SPACIROC within one EC had to be given up due to technical issues, the current design consist of an ASIC-Board, supplying six SPACIROCs with 36 MAPMTs.
As the main part of this master thesis is devoted to the development of a simulation board for this ASIC, the final version of the SPACIROC will be discussed in more detail in the following Sections.
The features of the SPACIROC3 are [19]:

- 64 channels of photon counting
- 9 channel Q-to-T Converter
- 100 % trigger efficiency for discriminating input signal greater than 1/3 photoelectron (p.e.) with 10 ns double pulse resolution at charges ≥ 50 fC
- Power consumption of 0.7 mW per channel
- 9 data serial outputs

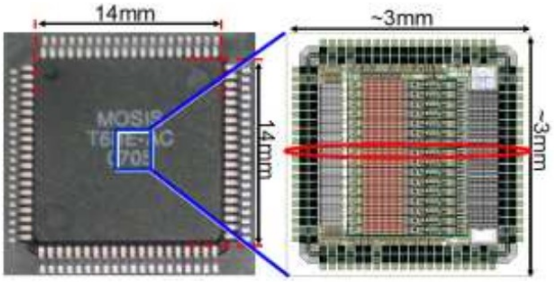


Figure 26 – The 80 Pin package (left) and the layout of the SPACRIOC (right). Image: [57]

Photon counting

The photon counting unit is designed to convert current signals from the 64 MAPMTs into trigger pulses parallel for each channel. The MAPMT anode-signal inputs are connected to the fast current preamplifiers which are based on the Super Common Base (SCB) structure of the MAROC3 ASIC [20]. The preamplfier has a variable gain rate combined with a low input impedance of ~ 100 Ohm in order to achieve less crosstalk. The current output of the preamplifier is transformed into a voltage by a ~ 5 kOhm resistor with a gain of 1.8 $\frac{\text{mV}}{\text{fC}}$. The discriminator transforms these voltages into trigger pulses. The threshold for the discriminator is calculated by a 10 bit common DAC register, and a second 7 bit individual DAC that compensates the MAPMT gain variation of each channel. The resulting trigger pulses are sent to the digital back-end of the ASIC. According to the scientific requirements of JEM-EUSO the trigger pulse width must be smaller than 10 ns which requires a very fast response of the preamplifier and the discriminator.

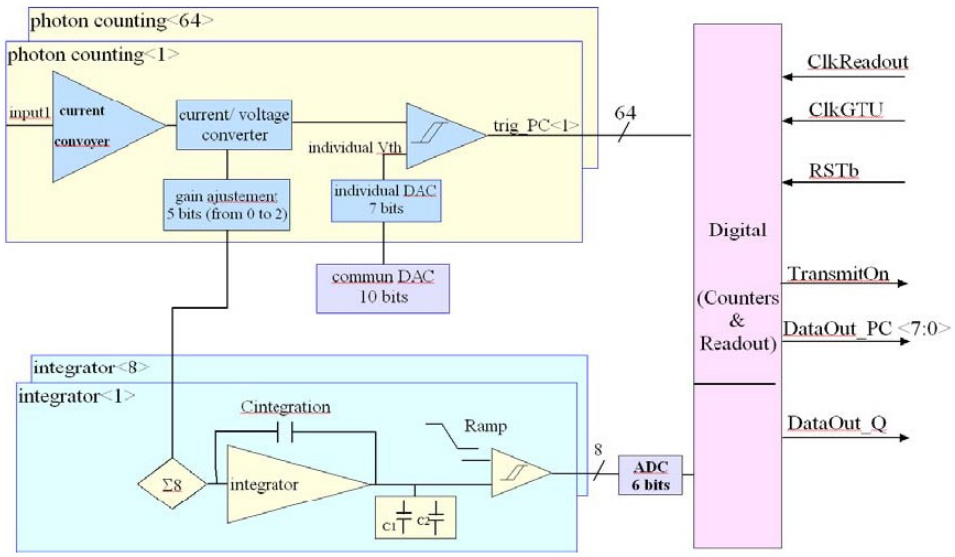


Figure 27 – The SPACIROC3 architecture with the photon counting block (yellow), the KI (pale blue) and the digital back-end (purple). Auxiliary components as the bandgap reference, the slow control register and the signals monitoring are not shown. Image: [19]

Charge measurement (KI)

The charge measurement unit of the SPACIROC produces a rough estimation value of the input charges of the MAPMT. The preamplified current from the PC unit first gets summed up from 8 consecutive channels and is then used as an input for 8 parallel integration amplifiers, which consist of a basic operation amplifier integration circuit with a feedback capacitor and resistor. Every single channel can be gain adjusted by 5 bit register before summation to account for the inhomogeneous gains per channel of the MAPMT. Additionally this register can be used to set a dynamic range for the p.e. rates per channel. Two capacitors serve as analog memory of the integrator output, which are switched in a "ping-pong" mode to avoid dead time caused by the 6 bit ADC, which converts the integrated charges and sends them to the digital back-end. The KI data indicates high average photon counts of the MAPMT and is therefore used for surveillance in order to protect the PMTs from overcharging. If critical values are reached the High Voltage is switched down for lower gains and the slow mode (see Section ???) is enabled.

Digital design

The digital part serves as a back-end for communication with the PDM. Its main parts are the 8 serial outputs for the 64-channel photon counting, the 6 bit output of the KI-data and the slow control communication bus.
The data read-out process has to finish within one Gate Time Unit (GTU) clock cycle (2.5 μs), which corresponds to a 400 kHz clock, while the system clock of the digital block is 100 times higher with 40 MHz. Both clocks are received from the PDM via dedicated Low Voltage Differential Signaling (LVDS) routes. 64 8 bit Gray counters are clocked by the trigger signals from the Photon Counting block. The resulting 512 bit counting data is sent by 8 serial output ports to the PDM. A parity bit originally implemented to check data integrity is currently not used for the present missions.
The KI-data from the eight 6 bit ADC gets sent via an serial output port, which sends the 48 bit stream for every GTU.
The slow control register allows to change basic parameters of the SPACIROC from the PDM, and is designed for maximum robustness towards radiation. Critical flip-flops are implemented

in Triple Modular Redundancy (TMR) configuration in order to achieve the rad-hard requirements.

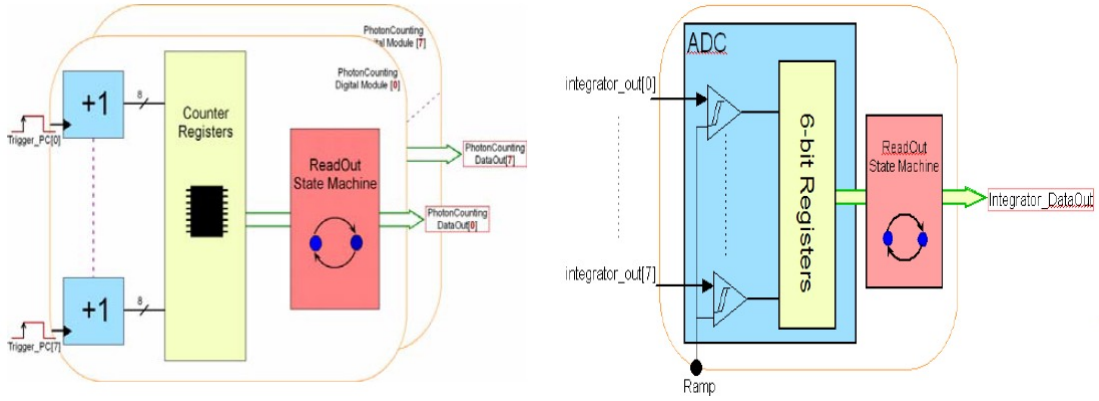


Figure 28 – Left: The digital Photon Counting module with the 8 serial output links, right: the digital 6-ADC output of the KI-data. Image: [19]

3.1.6 The PDM Board

The purpose of the Photo-Detector Module (PDM) board is to read-out and control the 36 MAPMTs of one PDM unit. Originally designed and produced at the Korean Ewha Womans University an updated version was developed at the IAAT in 2016. It is based on a Virtex 6 VLX365T Field-Programmable Gate Array (FPGA) manufactured by Xilinx. It is responsible for collecting the digital data from the 36 SPACIROCs, performing the first level trigger (FLT) (see Section ???) and sending the data to the CCB in case of a trigger event. Additionally, it receives configuration commands for the ASIC from the Mission Data Processor (MDP) and sends it to the SPACIROC. Depending on the received KI-data the PDM decides to switch between the fast mode for single photon counting and EAS observation and the slow mode for KI-data measurement used for asteroid, TLE and other atmospheric event observation.
The board receives the 40 MHz system clock from the CCB, derives the 400 kHz GTU clock and distributes both to the six ASIC-Boards, which are connected via 120 pin slots each, and the CCB. Every GTU clock cycle the PDM receives data from the 2304 single photon count channels and the 288 KI-data channels and stores them in a 128 GTU ring-buffer memory. Every GTU the FLT checks for signal persistency indicating an EAS. If an event is detected the data stored in the ring-buffer is sent to the CCB via a dedicated LVDS interface for further processing (for detailed information see the diploma thesis: Development of a PDM-Simulator Board for JEM-EUSO, by Gottschall 2013[21]). The improvements applied to the updated version of the PDM are mainly a new power supply system, that significantly improved the power efficiency, an updated housekeeping module, and a modified cooling system for the Virtex 6 FPGA, which tended to overheat in the basic version. The updated PDM board is shown in Figure ???.

3.1.7 The Cluster Control Board

The Cluster Control Board (CCB) is designed to further reduce the data rate and also act as an interface between eight PDM-Boards and the Mission Data Processor (MDP). The original design and manufacturing was done by Jörg Bayer at the IAAT in 2010[22].
The first working prototype was equipped with a Virtex 4 FX140 FPGA, while the CCB used for the EUSO-Balloon and the ESUO-SPB is equipped wit a Virtex 4 FX60 FPGA, both manufactured by Xilinx.

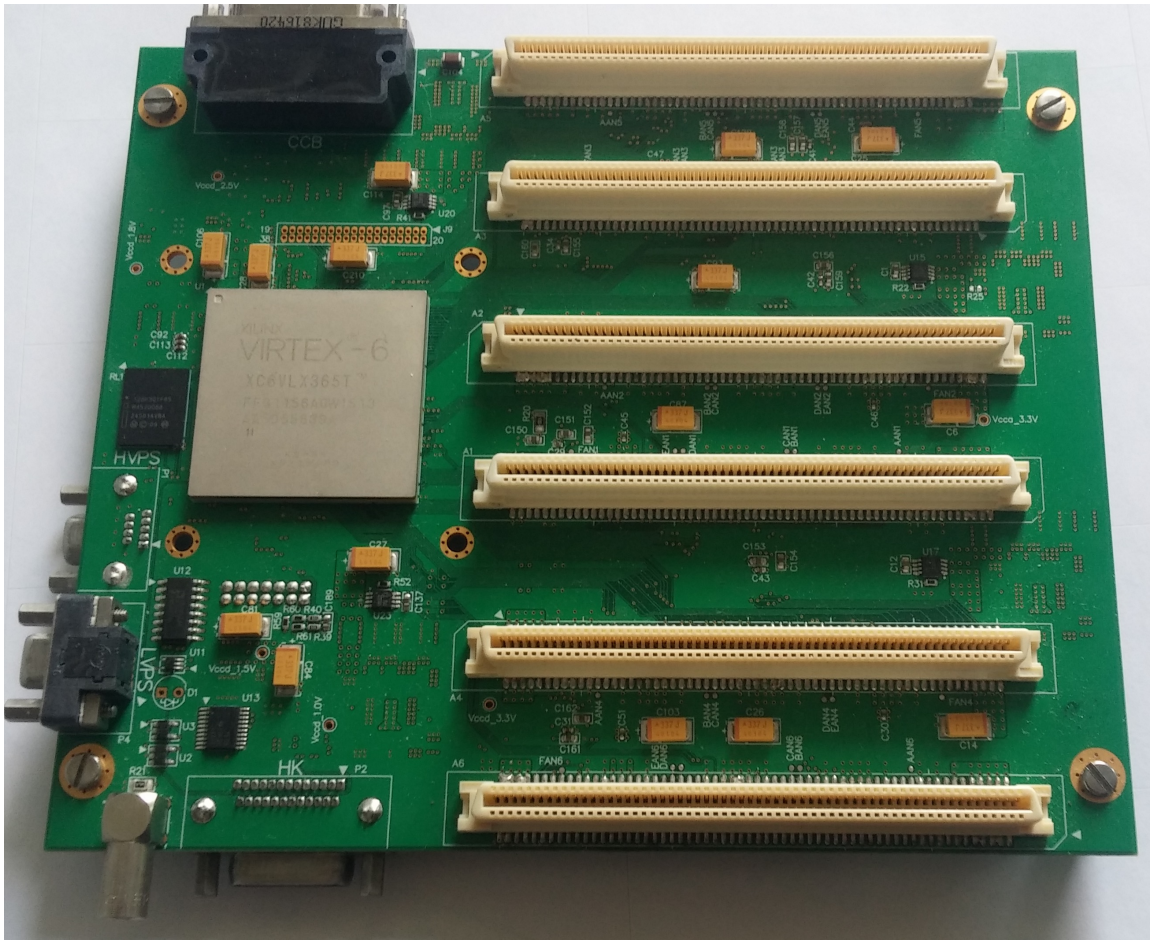


Figure 29 – The updated Photo-Detector Module Board with the Virtex 6 VLX365T FPGA on the left and the six 120 Pin ASIC connectors on the right.

The CCB also has a 40 MHz system clock, which is received from the MDP clock-Board. If one FLT of the PDM-Boards is activated, the data from the ring-buffers of all eight PDMs is transferred to the CCB and written to an external RAM. The CCB then performs the Level 2 trigger algorithm for each PDM data-block individually (see Section ???). If the L2 trigger is issued, the complete data from all eight PDMs is sent to the mass memory module of the MDP via the IDAQ communication block using the SpaceWire protocol.

3.1.8 The Mission Data Processor

The Mission Data Processor consists of a low power CPU, an IDAQ-board for the communication with the 18 CCB-boards, and clock-board for timing synchronisation. The system is composed of two redundant Storage and Control Units (SCUs).
The clock-board is responsible for generating the 40 MHz the system clock, the 400 kHz GTU clock and the synchronisation signal for all FS subsystems. Due to its connection to the GPS module it is able to set exact timestamps $\Delta t \leq 5\,\mu$s for individual trigger events. When it receives L2 triggers from the CCB the trigger-signal is passed to the CPU via the IDAQ interface and a busy signal is sent to the CCBs in order to stop data transaction until the event is processed by the CPU. The procedure allows life-time and dead-time measurements.
The IDAQ board receives the event data from the 18 CCBs and transmits them to the CPU via a PCI Interface. The communication between CCBs, clock board and IDAQ is realised with the LVDS standard and redundancy for all signals in order to keep the noise and the power

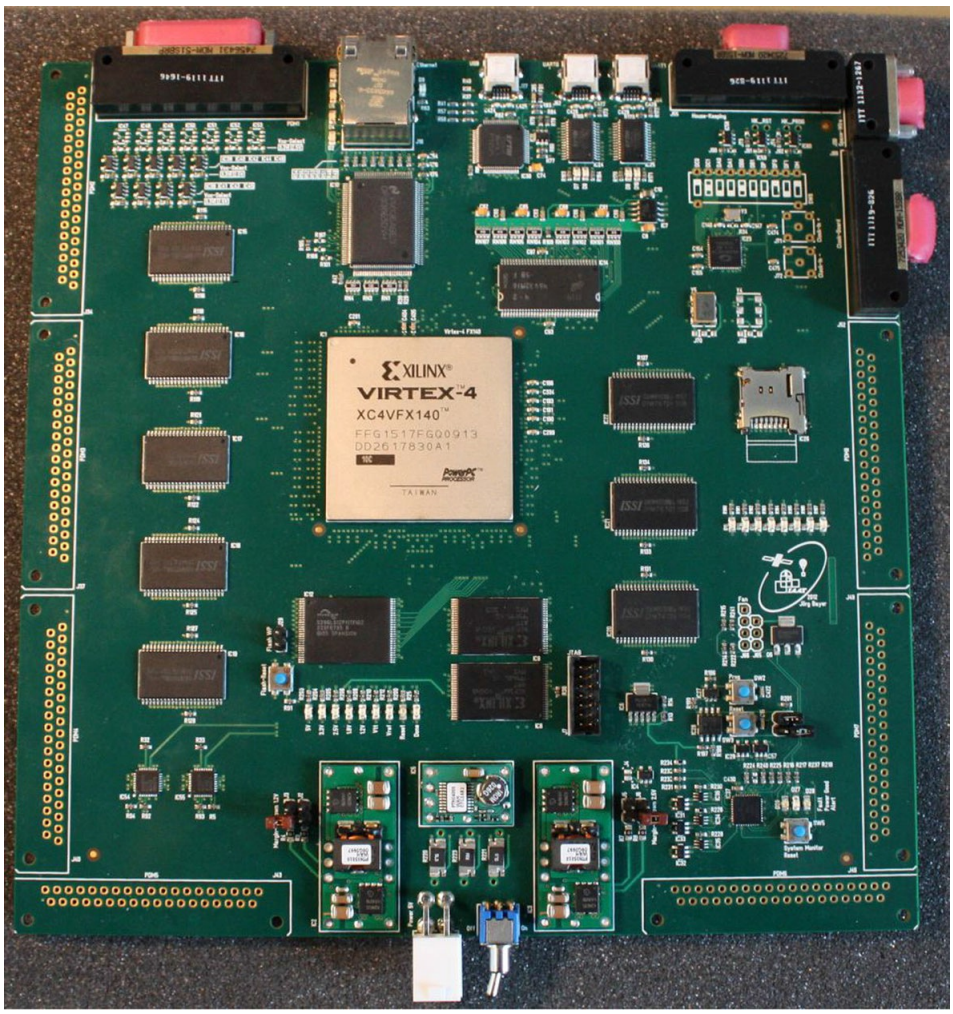


Figure 30 – The CCB prototype build at the IAAT. Image: [22]

consumption as low as possible while maintaining mechanical and thermal robustness.
The CPU controls the data acquisition of the whole instrument and establishes the communication to the ISS (for the JEM-EUSO mission) or the Tracking and Data Relay Satellites (for the EUSO-Balloon and the EUSO-SBP missions). Its main tasks are:

- Power control of all subsystems
- Acquisition start/stop
- Define trigger mode acquisition
- Periodic calibrations
- Control Housekeeping parameters
- Handle and pass (slow control) 1553 commands
- Take care of real time contingency planning

3.2 The Atmospheric Monitoring system

The Atmospheric Monitoring (AM) system provides information on cloud density, optical depth and coverage below the instrument during the observation time. The information will be used

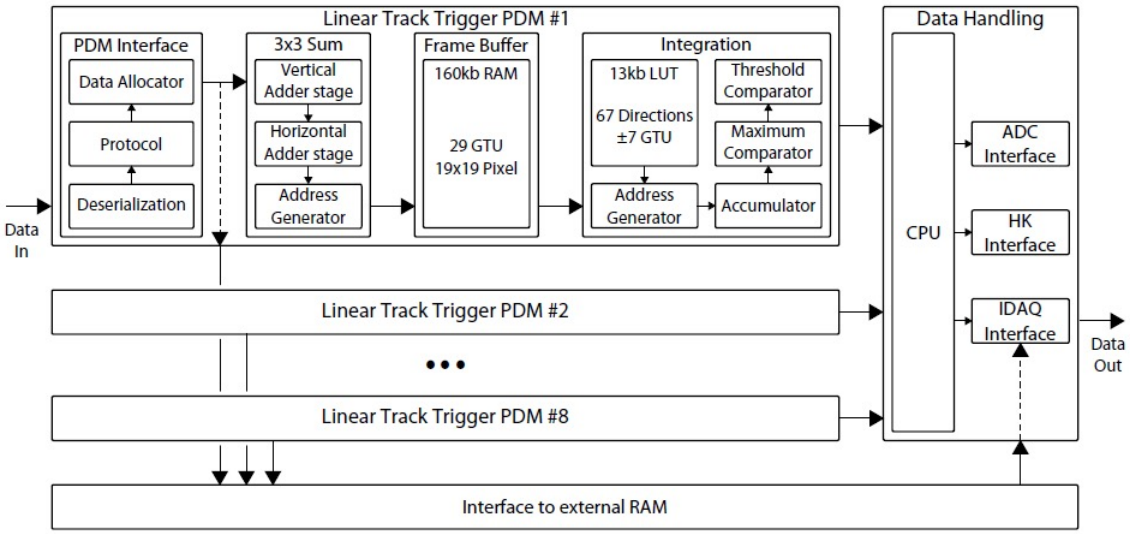


Figure 31 – The block diagram of the CCB FPGA. The linear track trigger module is implemented for each of the 8 connected PDM-boards. The external RAM is needed to store all the data from the PDMs as the FPGA Block-RAM memory is insufficient for the data size. The data handling is performed by internal microcontrollers of the FPGA. The IDAQ interface establishes the connection to the MDP. Image: [58]

in the offline data analysis to decrease reconstruction errors. The AM system consists of an infrared camera and a LIght Detection And Ranging (LIDAR) device[23].
The infrared camera will observe the cloud coverage of the entire FOV continuously, while the LIDAR is only activated by a trigger event and will measure the optical depth profiles at several locations around the detected EAS event. With the combined data for every event the optical depth τ will be categorized in three classes:

- $\tau < 0.15$ (clear atmosphere)
- $\tau = 0.15 - 1$ (thin clouds)
- $\tau > 1$ (thick clouds)

3.2.1 The infrared camera

The IR camera of JEM-EUSO is responsible for the detection of clouds and determination of their top altitude during observation of the main instrument. The IR emission of the clouds at night will be observed and the corresponding emission temperature can be used for the altitude calculation.
The FOV of the instrument matches the main JEM-EUSO telescope FOV and the angular resolution is $0.1\,^\circ$ per pixel. The instrument calibrates itself to an internal reference temperature and is able to compensate the background noise and gain of the detector for an absolute accuracy of $3\,\mathrm{K}$ [24].

Figure 32 – The mechanical structure of one SCU with removed panels. Image: [2]

3.2.2 The LIDAR

The LIDAR device will measure the scattering and extinction properties of the atmosphere around a detected event and between the detection area and the telescope and consists of a transmission and receiving system. The transition system is composed of a Nd:YAG laser and a steering mirror for controlling the laser direction.
The laser system has an operational wavelength of $\sim 355\,\text{nm}$ which is the third harmonic of the typical wavelength of $\sim 1064\,\text{nm}$ for Nd:YAG lasers. This shifting of the wavelength is achieved by a frequency-tripling crystal located inside the laser beam and is necessary to allow the JEM-EUSO telescope to serve as the receiving system as the timing properties of the backscattered laser shots are similar to the EAS profile. The system properties are shown in Table ???.

Table 2 – Specifications of the JEM-EUSOs LIDAR system. Table: [23]

Parameter	Specification
Wavelength	355 nm
Repetition rate	1 Hz
Pulse width	15 ns
Pulse energy	20 mJ/pulse
Beam divergence	0.2 mrad
Receiver	JEM-EUSO telescope
Detector	MAPMT (JEM-EUSO)
Range resolution (nadir)	375 m
Steering of output beam	$\pm 30°$ from nadir
Mass	14 kg
Dimension	$450 \times 350 \times 250$ mm
Power	< 20 W

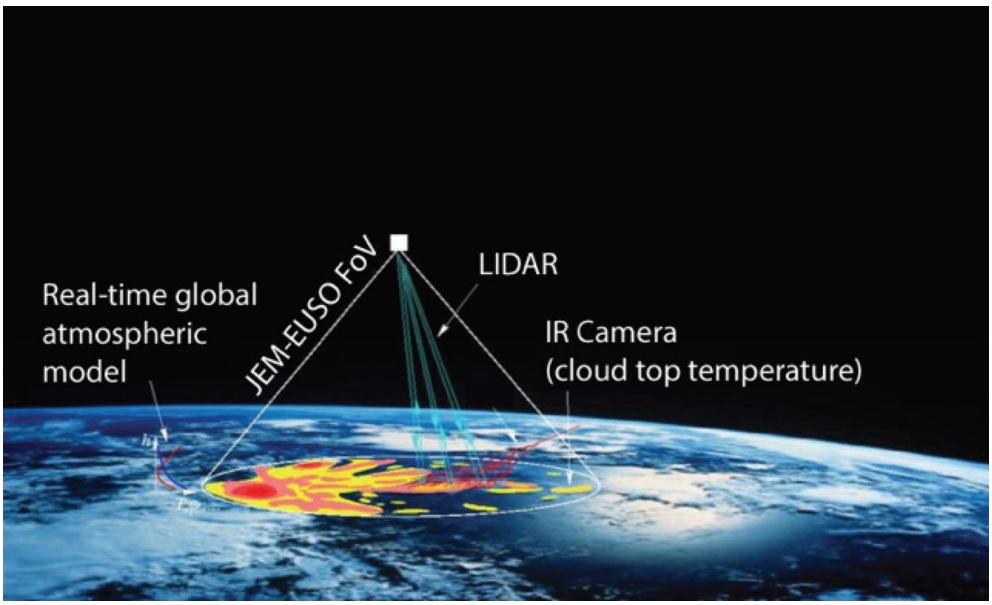


Figure 33 – Schematic picture of the Atmospheric Monitoring system. Image: [23]

4 The trigger system of the JEM-EUSO telescope

4.1 Overview

The trigger system of JEM-EUSO has to accomplish several challenging tasks: a) being able to process a large number of pixels (3×10^5); b) running on very fast, low power consuming, and radiation hard electronics; c) achieving a high signal to noise performance and flexibility (see Focal Surface requirements in Section ???); d) coping with the limited downlink transmission rate from the ISS to Earth [25].
The raw data amount of: 315×10^3 pixels $* 4 \times 10^5$ GTU $* 8$ bit/pixel ~ 1 TBit/s has to be reduced to the available downstream to earth. The maximum downlink is 3 GB/day [58], which means that a huge data reduction ($\sim 3 \times 10^6$) has to be performed in time in order to prevent data loss. To meet the data-budget requirement, the trigger system operates at two successive stages, reducing the data with different algorithms at each level. The First Level Trigger (FLT) is designed to operate at the EC level of the FS and is implemented on the digital part of the SPACIROC and the PDM FPGA. Its main goal is to reduce the fake trigger rate to ~ 1 Hz/EC. Fake triggers are mainly generated by random fluctuations of the night sky luminosity causing false coincidences. Also TLEs, meteors or man made sources like city light contribute to the fake trigger rate, when the instrument is switched to the fast mode (see Section ???).
The Second Level Trigger (SLT) operates at CCB level and is designed to identify tracks in the data sent from the PDMs. It reduces the trigger rate further to ~ 0.1 Hz/FocalSurface trying to distinguish the EAS typical pattern from the background. The complete architecture of the JEM-EUSO trigger design is shown in Figure ???.

4.2 The First Level Trigger

In this section the First Level Trigger (FLT) will be described in more detail as the redesign of the algorithm implemented on the PDM in order to meet hardware area restrictions is an integral part of this thesis. It filters a locally persistent signal lasting several GTUs above the threshold background value.

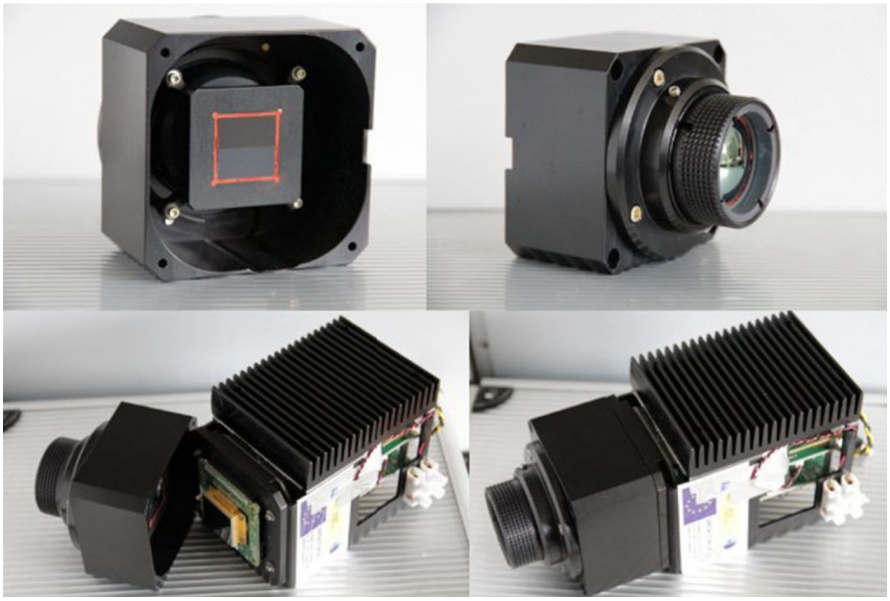


Figure 34 – Breadboard model of the Infrared camera. Image: [23]

The 1^{st} sub-level unit of the FLT is performed at the SPACIROC. The discriminator of the Photon Counting Block (see Section ???) acts as first noise suppressor and reduces the trigger rate to 1.4×10^{11} Hz/FS. Its detailed function is described above in Section ???.
The 2^{nd} sub-level trigger is implemented inside the FPGA of the PDM. The algorithm groups pixels in 3×3 boxes, with each inner pixel of a 8×8 MAPMT-unit belonging to a several cell, since the cells are overlapping. This results in one MAPMT hosting 36 cells. MAPMTs next to each other do not share cells. A pretrigger is set if at least one pixel per cell has a higher photon count than a preset threshold (N) for a certain number of GTUs (N_{ctd}) within a range of consecutive GTUs (P) and the integrated total photon count of the cell is above the threshold value (S). The presets for N_{ctd} and P are 3 and 5, respectively, while N and S are constantly changed by an average background calculation algorithm in order to keep the trigger rate constant at 1 Hz/EC. All parameters can be overridden externally during the mission.
The next step is to discriminate EAS events from other UV-light sources. An UV-light track of an EAS will hit the FS for less than 45 GTUs which is much shorter than the minimum duration of other events as lightnings (ms), meteors (hundreds ms) or cities and airplanes (seconds)[62]. Therefore, a confirmation counter is implemented which increments by 1 for every GTU in which the FLT is active for a preset number of consecutive GTUs (N_{GTU}). After N_{GTU} if the number of the confirmation counter exceeds the threshold (N^{thr}_{GTU}) the trigger does not activate as this indicates that the event is too long to be an EAS signature. The current presets for N_{GTU} and N^{thr}_{GTU} are 73 and 72. If the confirmation counter stays below N^{thr}_{GTU} a trigger is issued and the the data in the ring buffer is sent to the CCB.
For the average background calculation each EC is divided into 2×4 pixel groups. Every 128 GTUs the average photon count per pixel group is calculated, with the highest value determining the threshold values for the next 128 GTU cycle. The separation into 2×4 pixel groups is done in order to accommodate for the inhomogeneous behaviour of the pixels within one MAPMT and also to reduce the chance of an anthropogenic light source activating the trigger.

4.2.1 Implementation

The original trigger implementation was developed and tested in collaboration at the University of Torino, the University Catania and the INAF-IASF Palermo & Catania, Italy. A Virtex 6

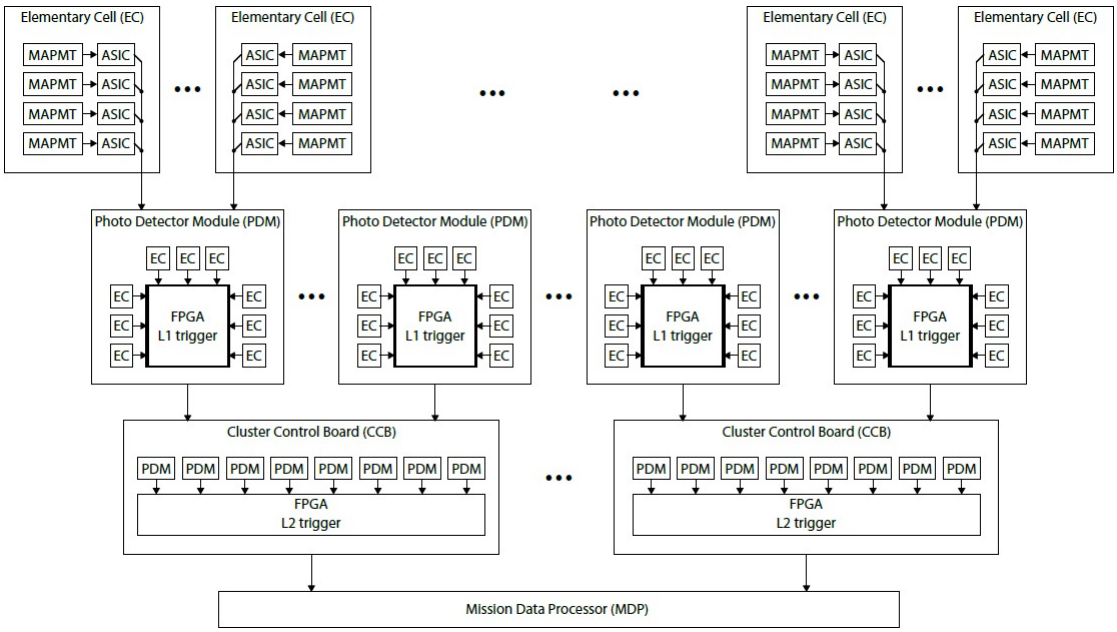


Figure 35 – Overview of the JEM-EUSO trigger architecture with the FLT operating at ASIC and PDM level and the SLT located at the CCB. Image: [22]

LX240T was chosen as FPGA target and later replaced with a Virtex 6 VLX365T in the course of the updated PDM design in 2016. The schematic of the trigger implementation with its different processes is shown in Figure ???.
The algorithm is organized hierarchically corresponding to the 4 MAPMTs per EC and the 9 ECs per PDM. For each MAPMT one VHDL-module called SPACRIOC (S1 - S4) is responsible for the pretrigger calculation and the background average calculation.
The SPACIROC module is composed of five processes:

- **Serial Pixel in to Column out (SIPO):** This process performs the read out and summation of the individual pixels for the 3×3 boxes. For every GTU cycle a 70-step state machine first samples each pixel column, compares each column pixelwise with the N threshold, and integrates the total photon count for each 3×3 box.

- **Memory GTU-Buffer:** The process is responsible for buffering the photon counts of the 3×3 boxes for several GTUs depending on the N_{ctd} value.

- **GTU SUM:** The GTU Buffer is sampled and summarized over the amount of P GTUs. The values are then compared to the R threshold and saved to another column array.

- **Check S:** The sum results from the GTU SUM process are compared to the S threshold in order to set the pretrigger for the MAPMT. The pretrigger event-data consisting of the the corresponding line and column, the photon count of the 3×3 box and the GTU number, is saved in a 24 bit First In First Out (FIFO) memory block.

- **Average Calculation:** The process summarizes the sampled pixels for each 2×4 pixel group, then consecutively compares the values of each pixel group while always saving the higher one. If the auto average calculation is enabled, the final value will be sent to the ALGO B top module.

The top VHDL module called ALGO B collects the pretriggers from the 4 MAPMTS and performs the persistency trigger calculation and the makes the final trigger decision. It also

receives the the average values for every MAPMT and calculates the new N and S threshold value for the next 128 GTU cycle. Its processes are:

- **Read FIFO:** In this process the pretrigger event-data is read out of the 4 FIFOs of the SPACIROC modules and stored in a single FIFO which will be sent with the ring buffer data to the CCB in case of the persistency trigger firing.
- **Average EC:** The MAPMT average values per GTU are compared to each other with the highest value saved for the threshold calculation.
- **Thr autoset:** The process receives the results of the Average EC calculation and averages them over 128 GTUs. The resulting new N and S threshold value is sent back to the SPACIROC modules.
- **S Trigger:** The pretrigger signals are collected and a flag signal is set indicating at least one pretrigger is in active state.
- **GTU count:** This process is responsible for the final trigger decision. It receives the flag signal of the S Trigger process and starts the confirmation counter. After N_{GTU} cycles a trigger is issued if the confirmation counter value is smaller than N_{GTU}^{thr}. The trigger signal is sent to the PDM top-module and is routed to the CCB from there.

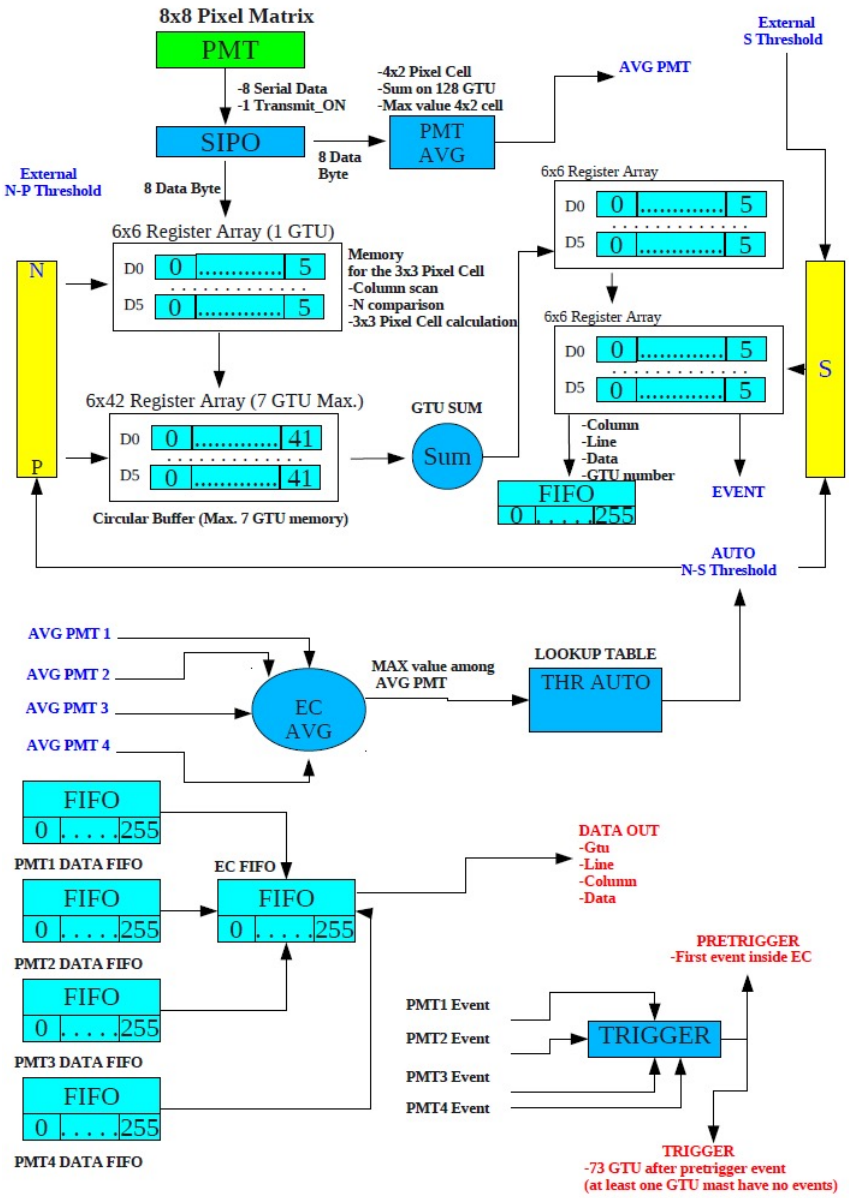


Figure 36 – Schematic of the hardware implementation of the FLT on the PDM FPGA. Image: [25]

4.2.2 Area Optimization

The original FLT VHDL design as described by M. Bertaina et al. in 2015 [25] already met all performance requirements and was tested extensively with various simulation data, but unfortunately exceeded the FPGA area constraints to allow the final integration on the PDM for the EUSO-Balloon mission in 2014.
One of the goals for the upcoming EUSO-SPB mission was the development of an updated version of the PDM with a working FLT that is fully integrated and tested. The different steps of improvements for the FLT hardware design in order to reduce its hardware utilization resulting in a final version which was integrated for the EUSO-SPB mission are described in detail in this section. First a short introduction in FPGA architectures is given to explain why these improvements were necessary and how they achieved achieved the goal meeting the FPGA resource restrictions.

FPGA architecture

FPGAs consist of programmable logic cells called Configurable Logic Blocks (CLB) and reconfigurable interconnects that "wire" the cells together. For most FPGAs the CLBs consist of Look Up Tables (LUTs), Flip-Flops e.g. latches which are called Slice Registers, and multiplexers. The number of LUTs and Slice Registers per CLB depends on the type of FPGA. While Slice Registers are only used to store signal states, LUTS can act as logic or memory depending on demand. Modern FPGA designs also feature dedicated memory blocks of static Random Access Memory (RAM) and Digital Signal Processing (DSP) cores distributed among and controlled by the CLBs. These usage of RAM and DSP blocks makes designs very area efficient as they are unlike CLBs specifically designed for the task.
A VHDL design first has to by synthesized and then can be mapped and routed on the available logic cells of the target FPGA. The mapping algorithm tries to find an optimal placement while meeting all timing constraints, which means no signal route can be longer than the distance the signal is able to travel within half of a clock cycle. If the timing constraints are not met, the function of the implementation can not be guaranteed. For complex designs with an area utilization above $\sim 60\,\%$ the algorithm might no more be able to find a mapping that fits on the FPGA while meeting all timing constraints. Additionally, even if the algorithm succeeds to find a valid mapping, the process will take extended time periods, making further development of the design heavily time consuming.

The 6.5 Version

In the paper: The First Level Trigger of JEM-EUSO: concept and tests, 2015 by M. Bertaina et al. [25] it is stated that for the 6.5 version of the FLT the algorithm of one EC requires $\sim 7\,\%$ of the FPGAs resources. As every PDM has to compute 9 ECs, this value would already go up to $\sim 63\,\%$ of the used resources for the FLT alone. While this version of the FLT passed all functional tests and showed good overall performance, its area utilization made it unfeasible for the PDM integration, considering that other VHDL modules as the ring-buffer, the CCB-interface, the housekeeping and the Top Module had to be integrated on the same FPGA platform as well.

The 6.5D Version

A considerable advance was made with the 6.5D version, in which a large part of the memory allocated for the FLT was now implemented on 18 Kb Blocks RAM cells instead of using

common LUTs. Also most of the summation operation used the dedicated DSP 48 bit cores instead of normal register logic. These measures resulted in a logic utilization reduction from $\sim 7\,\%$ to $\sim 4\,\%$ per EC but brought up another issue. One EC now consumed $\sim 10\,\%$ of the Block RAM resources, leaving virtually no Block RAM for the 128 GTU ring buffer.

The improved 6.5D Versions

The 6.5D version presented the basis on which the different steps of the area optimization were performed at the IAAT. The Table ??? shows the different versions with their area utilization per EC and for the complete FLT on one PDM. The first updated version 6.5D-1 reduced the required 18 Kb RAM Blocks form 85 to 13 per EC, which is a $\sim 85\,\%$ decrease in RAM utilization. The usage of Slice Registers decreased from 8231 to 6819, while the usage of LUTs was increased from 7096 to 7230. These improvements have mainly be achieved by serialisation of the Block RAM utilization in the SPACIROC modules. A new clock with 80 MHz was implemented for this purpose giving the SIPO, GTU SUM and Check S algorithms double the number of clock cycles to complete their tasks.

The second updated verison 6.5D-2 focused on reducing the amount of DSP cores as the original design utilized nearly the total available amount of DSP 48 bit cores. The result was a reduction from 80 to 52 DSP cores used per EC. Again serialisation of calculations using the faster clock domain enabled the improvement. After the decision was made to implement the Virtex 6 VLX365T on the updated PDM instead of the Virtex 6 VLX240T the utilization of the DSP cores had to be optimized further as the updated Virtex 6 VLX365T contains more Slice Registers and LUTs but 25 % less DSP cores compared to the Virtex 6 VLX240T.

The third version 6.5D-3 reduces the DSP utilization from 52 to 20 DSP-blocks per EC and therefore meets all area constraints. With some minor modifications this version was integrated on the PDM FPGA and passed all field tests in preparation for the EUSO-SPB mission.

4.3 The Second Level Trigger

The Second Level Trigger (SLT) also named Linear Track Trigger is responsible for identifying tracks in the data sent from the PDM and comparing them to a set of predefined directions in order to reconstruct a rough direction of the track. An EAS event is detected as a moving spot of light traversing over the focal surface. The track direction and length are therefore valuable information for the identification of the event parameters.
The trigger data contains the 128 GTU photon count data for every pixel of the PDM and also information about the position of the FLTs first appearance (see the check-S process in Section ???). This so called trigger seed sets the starting point for the SLT algorithm as it has to be part of the track due to its persistency for several GTUs. The algorithm integrates the 3×3 box values along the preset paths for a 7 GTU duration in each time direction. Then more boxes along the track are added for 15 additional GTU time frames. The result is a total photon count along each preset direction.
The global maximum is used to give a direction estimation and if the integrated photon count of the maximum is above a predefined threshold, the SLT is issued and the data is sent to the MDP.
In his diploma thesis Jörg Bayer compared the performance of the algorithm with 67 and 324 directions [22]. The so called *baseline* set of 324 directions is used for the offline analysis for

Table 3 – Area utilization of the different FLT versions. The usage of the Block RAM and the DSP cores was reduced significantly for the final 6.5D-3 version

Device logic utilization for the FLT				
Version	6.5D	6.5D-1	6.5D-2	6.5D-3
Slice Registers per EC	8231	6819	6815	6920
LUTs per EC	7096	7230	7231	7242
RAMB 18 Kb per EC	85	13	13	13
DSP 48 per EC	80	80	52	20
Slice Registers on VLX240T	74079/301440 24, 6 %	61371/301440 20, 4 %	61335/301440 20, 3 %	62280/301440 20, 7 %
LUTs on VLX240T	63864/150720 42, 4 %	65070/150720 43, 2 %	65079/150720 43, 2 %	65178/150720 43, 2 %
RAMB 18 Kb on VLX240T	765/832 91, 9 %	117/832 14, 1 %	117/832 14, 1 %	117/832 14, 1 %
DSP 48 on VLX240T	720/768 93, 8 %	720/768 93, 8 %	468/768 60, 9 %	180/768 23, 4 %
Slice Registers on VLX365T	74079/455040 16, 3 %	61371/455040 13, 5 %	61335/455040 13, 4 %	62280/455040 13, 7 %
LUTs on VLX365T	63864/227520 28, 1 %	65070/227520 28, 6 %	65079/227520 28, 6 %	65178/227520 28, 6 %
RAMB 18 Kb on VLX365T	765/832 91, 9 %	117/832 14, 1 %	117/832 14, 1 %	117/832 14, 1 %
DSP 48 on VLX365T	720/576 100 %	720/576 100 %	468/576 81, 3 %	180/576 31, 3 %

angular reconstruction by the EUSO Simulation and Analysis Framework (ESAF). The reduced set of 67 directions was also tested due to computing time and space restrictions of the hardware and shows a difference of ± 200 counts between maximum and average which is lower than the average pixel background for almost all events, which is shown in Figure ???.

While the implementation of the updated FLT represents the contribution of this thesis for the PDM development, the next Section will describe the ASIC-Simulation Board which constitutes the core part of this work.

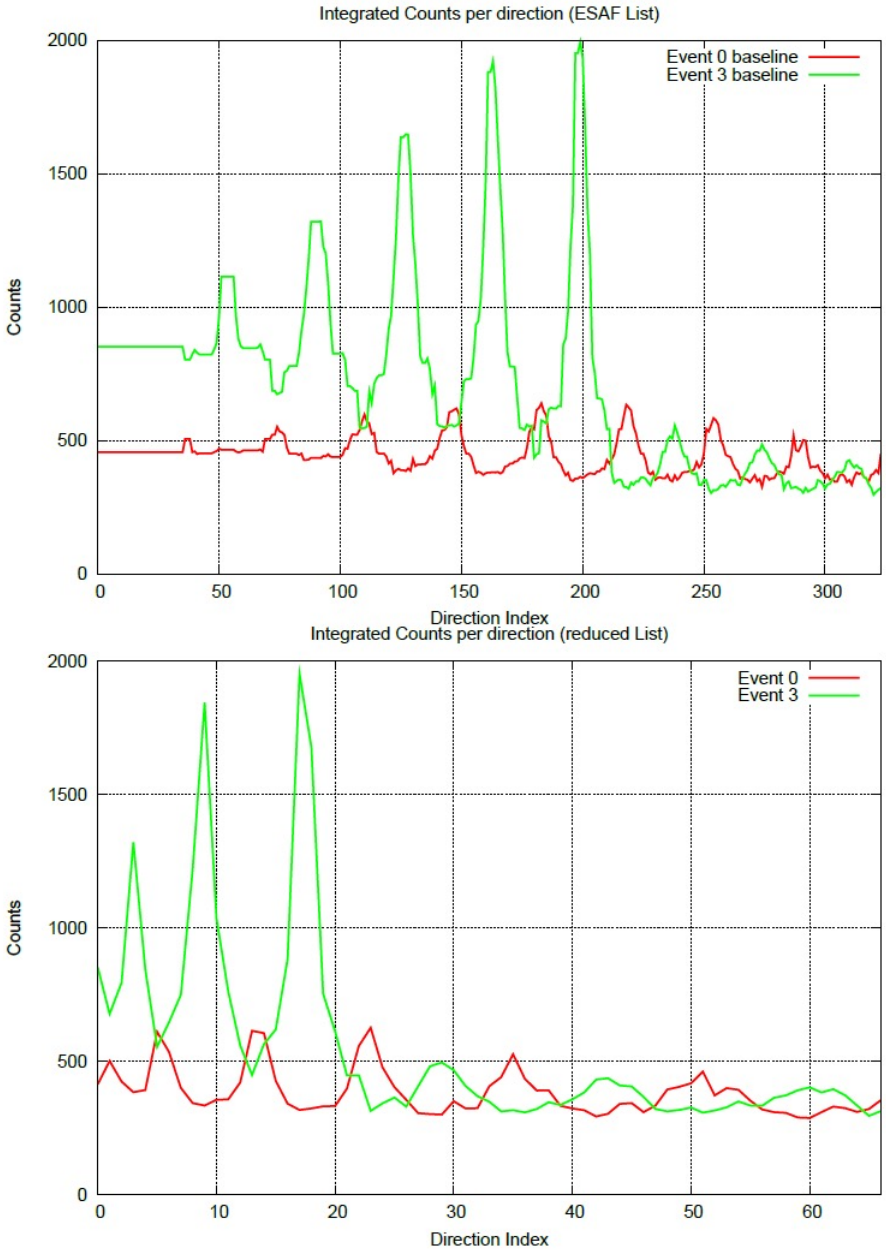


Figure 37 – Comparison between the 324 and the reduced 67 set of directions. The x-axis indicates the direction index, the y-axis the integrated photon counts per direction. The two colors represent two events with different energies, $1.39 * 10^{20}$ eV for event 0, and $3.92 * 10^{20}$ eV for event 3. The top image shows the response with the baseline set, the bottom image the response for the 67 direction set.The global maximum gives the most likely direction of the event. The occurence of other maxima can be explained due to the fact that for some directions the track is still partly inside the boxes. Image: [22]

5 The ASIC-Simulation Board

5.1 Overview

The development of the ASIC-Simulation Board (ASB) represents the main part of this master thesis. The PDM-Board has been developed at the Institut für Astronomie und Astrophysik Tübingen (IAAT) and the ASIC SPACIROC is developed at the Laboratoire de l'Accélérateur Linéaire (LAL) in France.
In order to test the full functionality of the PDM programming and interface to the SPACIROC for the upcoming ESUO-SPB mission the hardware had to be at the same place which made continuous testing of updated versions practically impossible. The ASB was therefore developed as a substitute for the SPACIROC hardware in order to simulate its functions and behaviour as close as possible. The test setup consists of the ASB, the updated Photo-Detector Module (PDM) hardware and the Cluster Control Board (CCB), as well as a CPU with a SpaceWire card as substitute for the Mission Data Processor (MDP).
For tests of the PDM interface and the complete trigger chain, the ASB uses the same hardware connector as the SPACIROC. MAPMT data packages can be sent from a PC to the ASB via a serial interface. The ASB stores and sends them to the PDM according to the parallel interface protocol of the SPACIROC. Figure ??? shows the data flow between computer, ASB components and PDM.
This section will give a detailed report of the components used for the ASB as well as its functionality and programming.

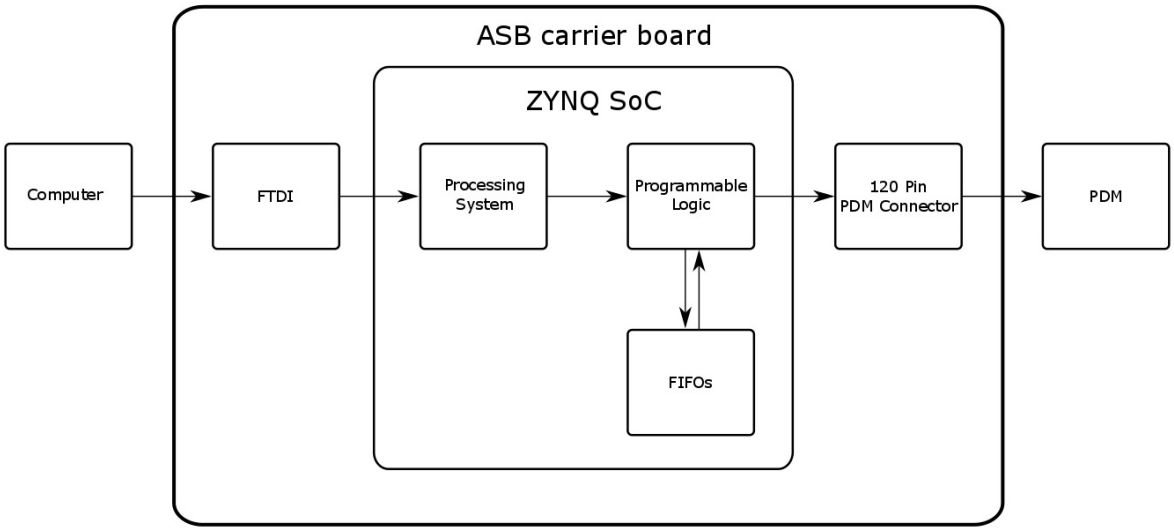


Figure 38 – The data flow of the ASB and its components. The test data is sent from a computer to the FTDI serial-to-USB-converter of the ASB carrier board (see Subsection ???). From there the data is fed to the UART module of the ZYNQ PS (see Subsection ???). The PL receives the data from the PS and stores it into six FIFOs, before sending it to the PDM (see Subsection ???).

5.2 Specification and Requirements

The main goal of developing the ASB was to have a programmable hardware substitute for the SPACIROC to allow continuous testing of the complete focal surface electronics and its data flow. Therefore the ASB should include:

- A connection to a computer to send test-data to it.
- Sufficient memory to store the received data and later create a constant data stream for the PDM.
- A large number of Input/Output (I/O)s required to emulate the parallel data interface to the PDM.
- Enough computing power to rearrange and grey encode the test-data before sending.

After the decision was made to use a Zynq SoC as main component to have the flexibility to develop the functionality on different levels and facilitate the programming tasks, the idea came up to expand the usability of the board also for project unrelated applications. Therefore, the hardware was implemented with an independent power supply and clock generation as well as several debugging tools, hardware switches and leds, which allow its usage as a powerful development board for a broad range of applications. Additionally, a small adapter board was developed to enable a free usage of the I/Os originally designated for the PDM interface. The fully assembled ASB is shown in Figure ???.

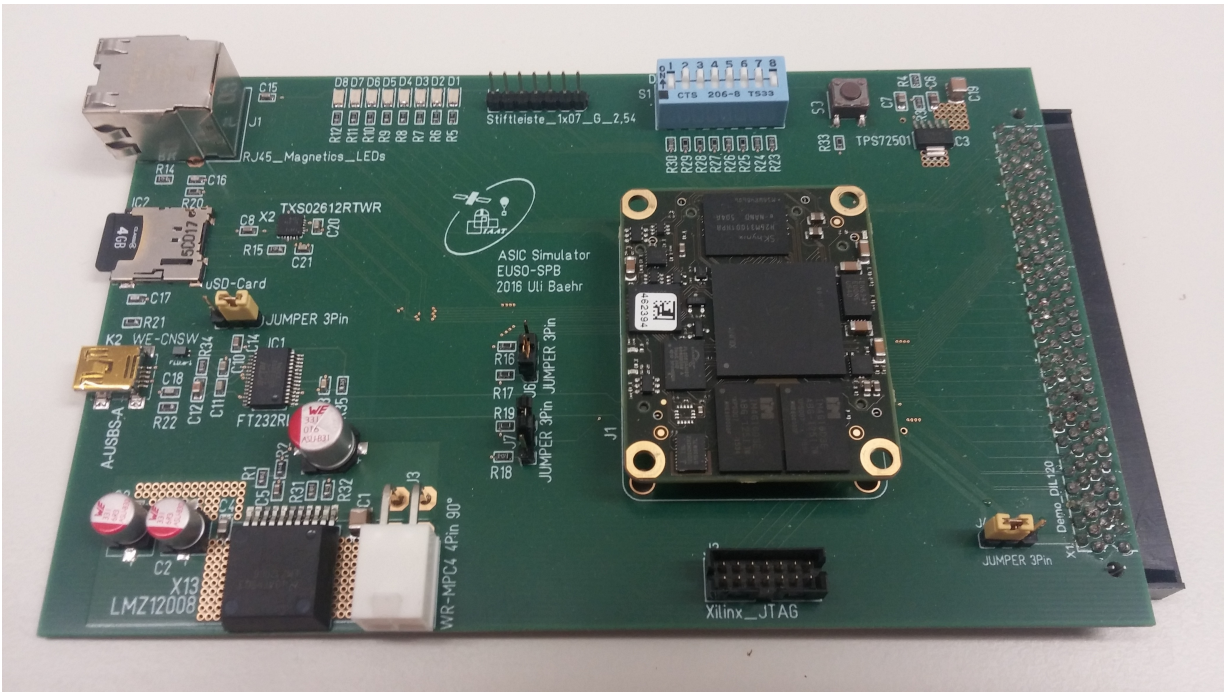


Figure 39 – The completed ASIC-Simulation Board with the Trenz TE0720 Zynq SoC module

5.3 The ZYNQ SoC

This chapter gives a short introduction to the architecture and functionality of the ZYNQ SoC manufactured by Xilinx. This product integrates a dual core ARM®Cortex™-A9 MPCore™based Processing System (PS) and Xilinx Programmable Logic (PL) in a single device. It also provides on-chip memory, external memory interfaces and a variety of I/O peripherals [26].
While the processors of the PS can either be programmed as bare metal application with the programming languages C/C++, it is also possible to run an embedded Linux operating system with an own file system on them instead. Xilinx provides a eclipse based development environment called Software Development Kit (SDK) for this purpose [61], but it is also possible to

program the PS with a different C/C++ compiler software.
The PL hardware is programmed with VHDL similar to common Xilinx FPGAs. With the launch of this new product family Xilinx also provided a new software framework called Vivado Design Suite for programming and debugging of all Xilinx product families released later than 2012 [60].
The main differences to its predecessor ISE Design Suite are the new block design and the integrated debug functionalities. The block design functionality provides a graphical overview of the VHDL toplevel and allows a fast integration of new ip-cores by simply adding them to the block design and connecting their ports automatically to a large extend. This new function not only gives a better oversight over complex VHDL projects by showing all connections and interfaces of different modules, it also allows the reconfiguration of ip-cores and the ZYNQ PS without having to manually change the port descriptions.
The system architecture is illustrated in Figure ???. The PS and the PL are on separate power domains, allowing the user to power down the PL for power management if necessary. The central interconnect is located in the PS domain and responsible for the connection of all I/O peripherals and interfaces and the both processing units as well as the PL. Additionally the the PL is connected to the PS by several high performance ports, which are directly connected with the memory controller and can be used for a fast transfer of large data packages. The clock generation and the reset network is both located in the PS domain and distributed from there. The common I/Os are connected to the PL but a part of them can be declared as General Purpose I/Os (GPIO) for direct connection to the PS. A 12 bit ADC is also provided in the PL domain.
The ARM®Cortex™-A9 MPCores™have a fixed system clock with 666.7 MHz from which four PL clocks with a frequency between 0.1 MHz and 250 MHz can be derived directly. The system boot of the ZYNQ SoC requires a precise power sequencing in order to start correctly. This function is provided by the Trenz micro module which is described in the next Section.

5.4 The Trenz TE0720 SoC micro module

The Trenz TE0720 micro module represents the core of the ASIC-Simulation Board.
It integrates the following modules on a 4×5 cm PCB:

- A Xilinx Zynq Z-7020 SoC.
- A Gigabit Ethernet transceiver (PHY) including a MAC Adress EEPROM.
- A 1 GByte DDR3 SDRAM module with 32 bit width.
- 32 MB QSPI Flash memory for configuration and operation.
- An USB ULPI transceiver for USB connection.
- The so called System Management Controller (SC) responsible for the necessary power-sequencing for the SoC boot.
- 166 Board to Board I/Os for free assignment.

Several reasons led to the decision to use this module and design a carrier PCB around it. First of all it brought a feasible solution for the integration of the SoC on the carrier PCB due to its 3 Samtec LSHM connectors on the bottom side, which made the manufacturing process of the carrier PCB significantly easier. The module also takes care of the complicated power-sequencing for the ZYNQ SoC, which would have been another problem to solve for a directly implemented SoC. It additionally provides sufficient memory with the two integrated 512 MB

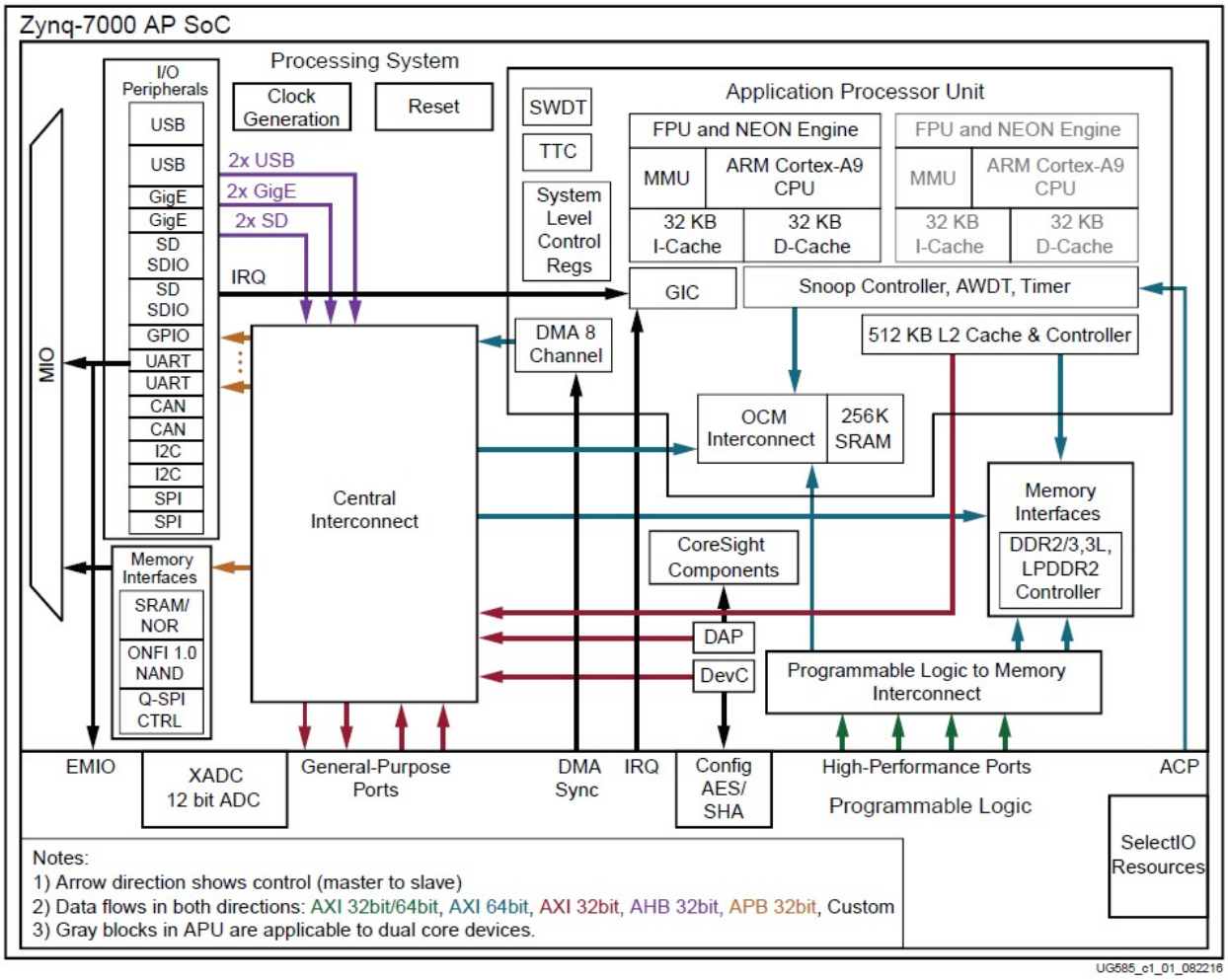


Figure 40 – ZYNQ SoC is mainly composed of the following functional blocks: The Processing System (PS), with the Application processor unit, the Memory interfaces, the I/O peripherals and the Interconnect. The Programmable Logic (PL) with the I/O resources and the XADC. Image: [26]]

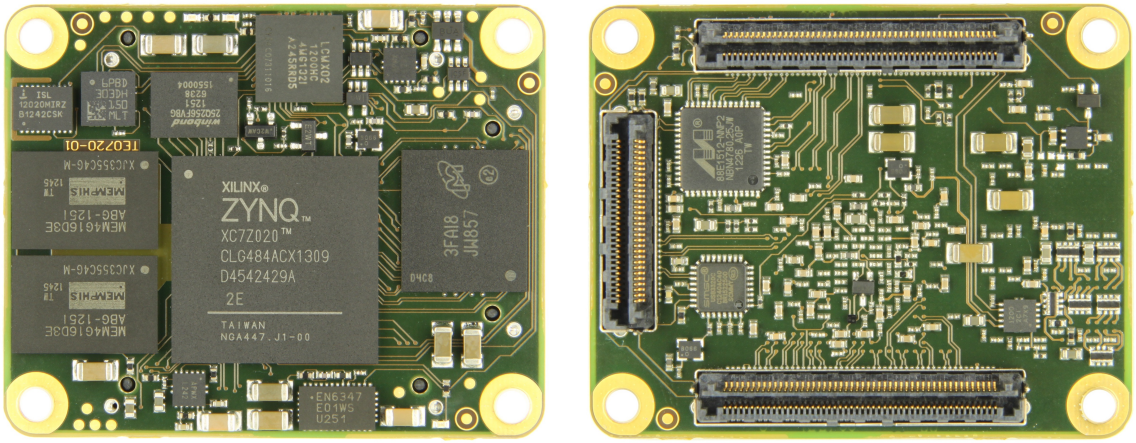


Figure 41 – Trenz TE0720 micro module: The imgage on the left shows the top view of the module. The Zynq SoC is soldered in the center with the two 512MB SDRAM modules left to it, the System Controller CPLD directly above it and the SPI flash memory between the SDRAM modules and the CPLD. The picture on the right is the bottom view with the Ethernet PHY in the top left and the Samtec Board to Board connectors on the top, left and bottom. Image: [70]

SDRAM modules and includes a reset system for all components. Its top and bottom view is displayed in Figure ???, while Figure ??? shows its basic architecture. The next Section gives a detailed report about the carrier board and its components.

5.5 The carrier board

The objectives for the carrier PCB are to provide a stable power supply for all board components, a USB, an Ethernet and a JTAG programming connector, and to route the necessary number of I/Os from the micro module to the PDM connector. It is additionally equipped with 8 LEDs, free I/Os and switches for simplified debugging purposes, a global reset button and a SD-card reader for automatic booting.
The board consists of four copper layers where the top and bottom layers are used for signal routing, while the inner layers are for ground and 3.3 V distribution. In the center the Board to Board connectors (J1, J2, J5) to the Trenz micro module are placed, which is powered by twelve 3.3 V pins. The standard JTAG connector used for programming the Zynq SoC is placed directly below the micro module (Xilinx-JTAG) and connected to the right of the three Samtec connectors (J2). Its circuit diagram is shown in Figure ???
On the right edge of the board the 120 pin PDM-connector (X1) is placed bottom sided. It is a right angle header FX2 connector type which establishes the connection between PDM and the carrier board. The 1.5 V supply voltage for the parallel 48 pin data bus to the PDM is provided by five pins at the bottom. Alternatively, a 1.5 V linear power supply (IC3) can be used as supply for the parallel bus. The jumper (J4) next to the PDM-connector is responsible for selecting one of the two power sources. The jumpers at the left of the PDM-connectors are for switching the boot-mode of the Zynq SoC between SD-card or QSPI Flash (J6), and selecting the JTAG mode of the micro module (J7).
The global power supply (X13) for the board is located in the left bottom corner of the PCB and generates 3.3 V with 8 A maximum current, its composition is described in detail in the next Section.
A mini USB connector (K2) and an FTDI chip (IC1) for converting the USB protocol into

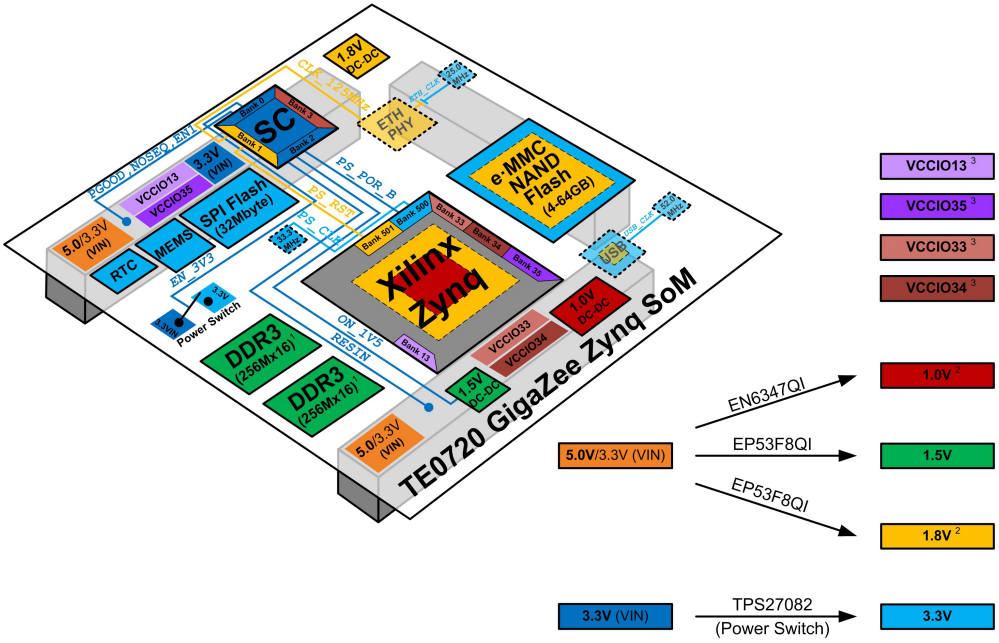


Figure 42 – The architecture of the Trenz TE0720 showing the system management, the power supply and the resets. Image: [70]

UART are located above the power supply. The jumper (J5) next to it is used for selecting the power source of the FTDI chip (all jumper functions will be listed in detail in Section ???). Above them an SD-card reader (IC2) with a level shifter (X2) are soldered at the left border of the PCB next to the Ethernet connector (J1) above them. All the interface connectors are described in detail in Section ???.
At the top of the board the eight LEDs (D1-8) , the seven free I/O-pins (K1), and the eight Switches (S1) are soldered next to each other and connected to the 60-pin top connector of the micro module (J5).

5.5.1 Power Supply

The power supply‘s main task is to deliver a stable 3.3 V supply for different input voltages and thermal conditions. It additionally protects the carrier board from over- or under voltage and short circuits. For these tasks, a LMZ12008 step down power module from Texas Instruments was selected. It allows an input voltage between 6 V and 20 V which increases the flexibility since no accurate laboratory power source is needed for running the board. An angled 4-pin connector is used as input power plug and located directly next to the LMZ12008. In order for the LMZ12008 to maintain the 3.3 V a feedback current loop is needed. Additionally several capacitors are necessary at the input and output sides to handle ripple currents and suppress high frequency noise. As all these components have to placed as close as possible to the LMZ12008 to prevent unstable behaviour, the PCB design of the power supply is directly oriented on the suggested design in the LMZ12008 data-sheet. An array of heat sinking vias is located under the copper pad of the converter to connect it to the ground plane in order to keep the junction temperature below 125 °C. The wiring diagram of the power circuit is shown in Figure ???.
During commissioning the supply has been tested with different input voltages from 5 V to 16 V and showed a satisfying performance (see Section ???). Also the short circuit protection was tested before the micro module was assembled. This test should not be repeated due to the load switches of the micro module which endure significantly less current than the 8 A of the LMZ12008.

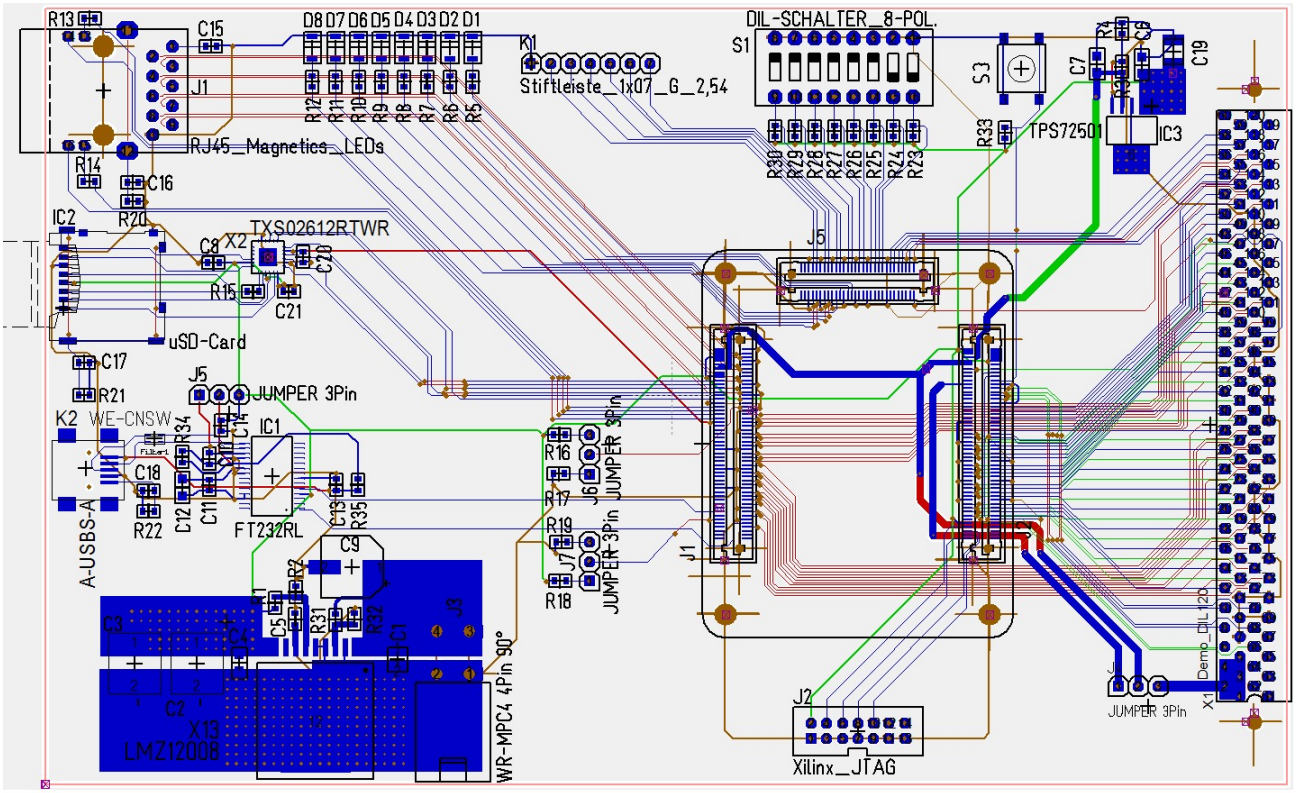


Figure 43 – Circuit diagram of the carrier board for the ASIC Simulation Board. The carrier board consists of four layers which are represented in different colors. The blue layer is the top layer. It is mainly used for signal routing and the power supply components. The second signal routing layer is the bottom layer and red coloured. It is used for connecting the left micro module connector to the PDM-connector and the Ethernet socket. The ground layer is used to distribute a common ground signal for all components and all screws and shieldings as well are connected to it. The green layer routes the 3.3 V supply to all components and connects a few signals, which could not be routed via the blue or red layer due to area restrictions. In a final step, copper planes are inserted for both 3.3 V and ground layers in order to reduce crosstalk between the signal layers and provide a large enough copper area for transmitting high currents. The black contours show the locations of the used components.

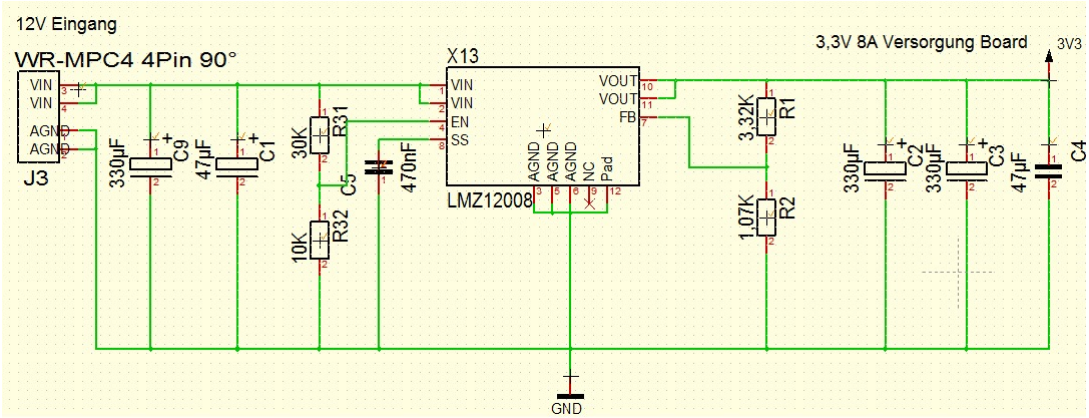


Figure 44 – The wire diagram of the carrier board power supply with the 12 V power connector on left and the 3.3 V output on the right.

5.5.2 Onboard Functions

With the possibility to implement a wider range of applications on the ASIC-Simulation Board in the future, eight LEDs and switches were implemented for debugging purposes. Both are connected to the micro module and can easily be used either in the VHDL design at Programmable Logic (PL) level or in the C-design at Processing System (PS) level. A seven pin connector enables the free usage of I/Os without the adapter board. The left pin of the connector is connected to ground and therefore provides an easy to access ground point for measuring purposes.
A global reset button allows the reset of all components on the micro module simultaneously and forces a reboot of the system. The program for PL and PS can be stored in two different places, either on the QSPI Flash memory of the micro module or on an external microSd-Card which has to be plugged into the card reader of the carrier board.
Four jumpers allow different configurations of the carrier board:

- **Jumper J4** is responsible for switching the 1.5 V power supply of the parallel bus between PDM and carrier board. 1-2 configuration uses the LDO supply located on the carrier board, while the 2-3 configuration uses power coming from the PDM via the 120-pin connector.
- **Jumper J5** switches the power supply of the FTDI chip between internal and 3.3 V rail. 1-2 configuration uses the internal power pin of the FTDI, while 2-3 configuration uses the 3.3 V supply of the carrier board. The 2-3 configuration is recommended as internal supply can lead to unstable behaviour.
- **Jumper J6** is responsible for boot-mode selection. 1-2 configuration corresponds to booting from the microSD-Card, while 2-3 corresponds to booting from the QSPI Flash.
- **Jumper J7** selects the JTAG-Mode. In order to let the Zynq SoC appear in the JTAG-chain the 2-3 configuration has to be selected.

5.5.3 Interfaces

The ASIC-Simulation Board supports several interfaces for communication with an external PC, such as Ethernet, UART via USB and JTAG. The JTAG debug interface is utilized for programming the Programmable Logic (PL), as well as the Processing System (PS) of the SoC. It also supports several debug functions for the PL, the PS CPUs and the internal analog digital converter (XADC) and allows the user to program the QSPI flash memory [26]. As the JTAG interface establishes a direct connection to the PS via the debug access port (DAP) and the PL via the test access port (TAP), there is no PHY involved and therefore no additional hardware implementation necessary besides the standard Xilinx connector.
The Gigabit Ethernet interface was originally planned to be the pathway for the large simulation data packages sent by a PC to the SoC. Its PHY is located on the Trenz micro module and is connected via four LVDS pairs to the RJ45 connector on the carrier board. Unfortunately during the soldering process of the surface mounted 100-pin Samtec connectors, one of the LVDS pairs was bridged directly under the connectors (see Figure ???). The removal of the Samtec connector would have likely resulted in a damaged board, with no possibility of reapplying a new connector on the same solder pads. This led to the decision to leave the board untouched as all other board tests went successful and implement the data transfer on the UART interface instead.
The UART interface was originally planned for software debugging of the PS by sending print commands directly in the code to a generic serial port terminal at the user PC. For guaranteed compatibility, a mini-USB connector and a serial-to-USB-converter in form of an FTDI

FT232RL chip were implemented, as most modern computers do not possess a RS-232 serial connector any more. The FT232RL is connected to the dedicated RX and TX Mixed Input/Output (MI/O) pins and can also be configured via the UART.

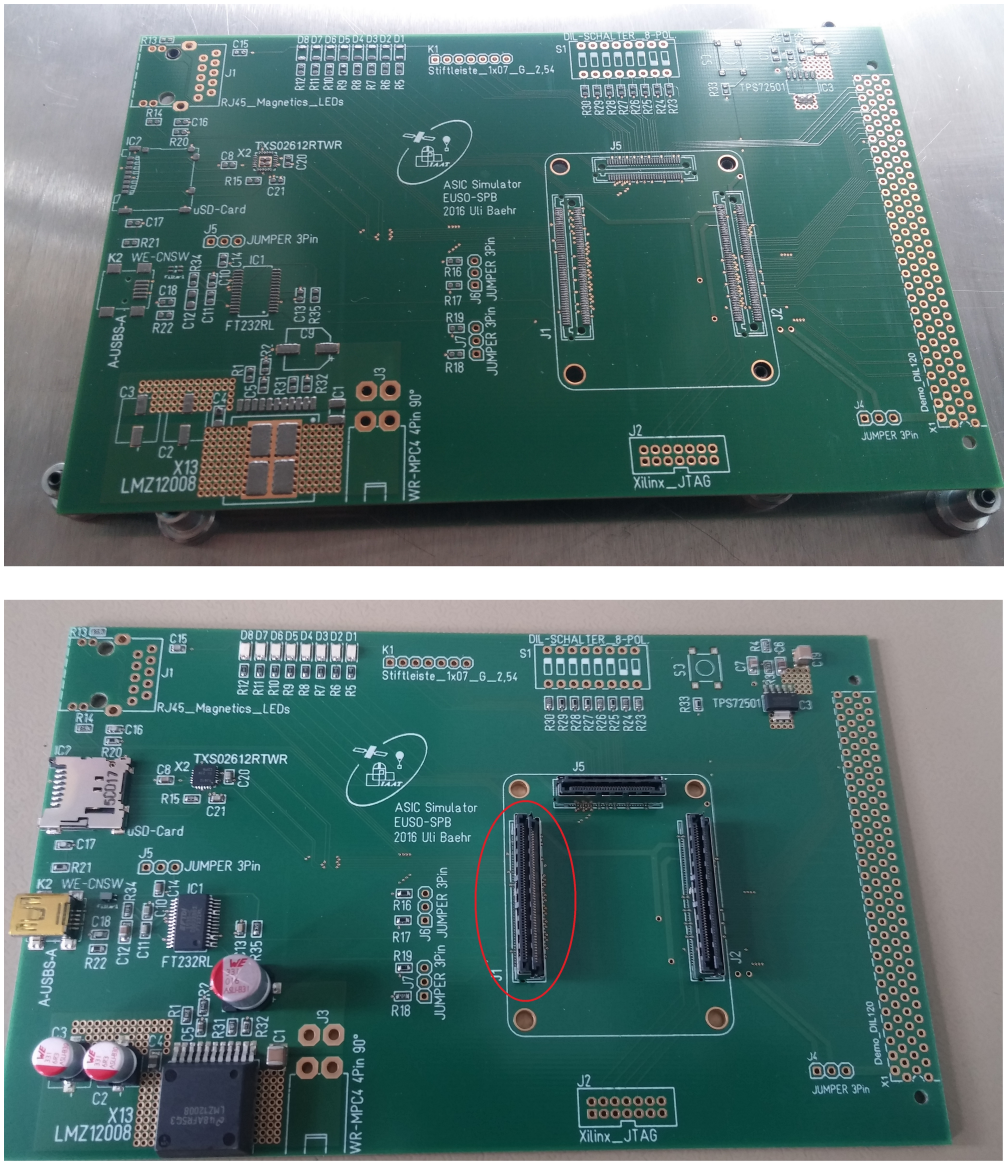


Figure 45 – The carrier board before the assembly at the top and after the assembly at the bottom. The damage on the Ethernet LVDS pairs was most likely caused by too much solder paste at the pads of the left Samtec connector, which resulted in two bridged pins after the soldering process.

5.6 Software Design

5.6.1 Overview

This section describes the implementation of the Processing System (PS) of the SoC and the functionality of the Python module used to send test-data from the computer to the PS. The PS is used as a bare metal application with no underlying operating system or file system and the software written in C using the *XILINX* Software Development Kit (SDK). The Xilinx System Debugger (XSDB), which establishes a scriptable command line interface to the hardware-server of the PS was utilized for debugging and memory checking.
The main tasks for the PS were to establish a UART connection to the user PC, transform the

data from ASCII-Code to hexadecimal, grey encode and finally send the data packages to the PL.

5.6.2 UART Interface

The UART Interface was originally planned for debugging purposes only, but as already mentioned in Section ??? it had to be used for data transaction instead. With a maximum baud rate of 115200 Bit/s its transaction speed is not as fast as the Ethernet standard but still sufficient for the task. On the PC side a Python module called pySerial [27] was employed, which encapsulates the access for the serial port and provides the backend for Python for all common operating systems. As soon as the operator starts the program, a specified text-file containing the test-data will be read by the module and sent ASCII encoded to the PS of the SoC.
On the SoC side the UART implementation is based on a driver example of the Board Support Package (BSP) for the UART module of the PS. The driver controls the function of the UART module and its control logic, sets up interrupts for the PS CPUs and controls the UART reference clock, which generates the baud rate. Its block diagram is shown in Figure ???. Once the communication port is opened and the connection is established, the transmitted data is stored in a FIFO memory block. Every data package has the unsigned 16 bit format and contains the photon count of one pixel, which is split up between the high byte carrying the first 8 bits and the low byte carrying the last 8 bits. So for one EC with 256 pixels the transaction will take 35 ms which results in a total transmission time of several minutes for an average simulation-data package containing several thousand ECs.

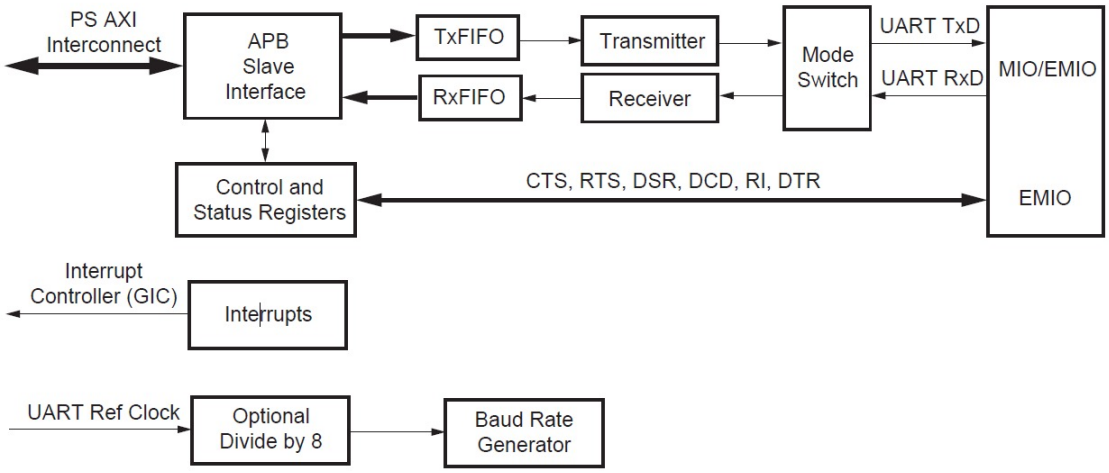


Figure 46 – The UART module block diagram showing the data flow from the mixed I/Os (MIO) to the PS. In the application utilized for the ASB, the transmitting direction was only used for early testing of the interface.
Image: [26]

5.6.3 Data encoding

Before the data can be sent to the PL, it has to be converted from ASCII to grey code. This task is done in two steps. First the data has to be encoded in to the standard hex format by subtracting 48 from the high byte and low byte of one data package and then rearranging both bytes to one packet again.
The idea behind this step is that numbers from 0 to 9 are encoded from 49 upwards in the standard ASCII table, so by subtracting 48 the original values are recovered. This conversion only works as long as integer values up to 255 are sent, which is sufficient, as the pixel counts

above 100 are not expected. The output hex values are then converted into grey code. The algorithm performs an nor comparison followed by a bitshift to the right of a given value a:

$$a_{grey} = a \wedge a >> 1 \tag{21}$$

5.6.4 AXI4 Interface to the Programmable Logic

The connection between PS and PL is established by simple read and write commands on the DDR RAM of the micro module via one of the AXI4 general purpose ports, which is possible due to the slow transaction speed of the UART. The Section ??? will give a precise description of the AXI4 standard and the different internal data ports. The most basic approach however is to write single data values directly onto a certain AXI4-slave address of the RAM and set a flag for new data. The master interconnect for the AXI general purpose ports of the ZYNQ will then take care of the RAM handling and management without further implementations required. The RAM addresses are managed on the PL for every module and a parameter set with the corresponding addresses is generated for the PS, on which the read and write commands can be referred to.
For every fetch cycle of the UART module, the software writes one converted photon count value onto one AXI4-slave port, and sets a "transaction finished" flag after the last value has been transmitted, which triggers the sending process of the data to the PDM.

5.7 VHDL Design

5.7.1 Overview

The firmware for the PL is written in VHDL using the *XILINX* Vivado Design Suite which is the successor of the Integrated Software Environment (ISE) and introduces a new graphical overlay of the top level VHDL design including port descriptions and configuration blocks for ZYNQ devices. It also integrates the former debug environment Chipscope into the toolchain and adds virtual IOs as an additional debug feature.
The main task implemented on the PL is the data handling of the received data from the PS using buffer FIFOs and emulating the parallel data bus of the SPACIROC-PDM interface. The design also takes care of the buffering and distribution of the system- and GTU clock and the generation of an independent internal clock network for standalone applications.

5.7.2 Clocking

The 40 MHz system clock and the 400 kHz GTU clock are received via LVDS signals from the PDM. In order to generate a logic clock signal for the design, two buffers per clock are implemented. The first is a standard LVDS buffer which buffers the two LVDS signals followed by one utility buffer which converts the signal into a standard clock signal. The second buffer is necessary as Vivado would not allow a common signal to be used as global clock without an independent buffer. Both buffers are configurable IP-Cores from the Xilinx core library.
In order to enable testing of the ASB without the connected PDM, it was necessary to also implement an internal system clock. The ZYNQ SoC provides four configurable clocks called fabric clocks for the PL which are derived from the 666 MHz clock of the PS CPUs (see Section ???). The internal GTU clock is generated by a custom VHDL module which divides the system clock by 100 as the common clocking wizard IP-core only allows derived clocks with a minimum of 1 MHz. The clock source can be switched from external to internal by one of the hardware switches of the ASB for convenience. The architecture of the clocking module is shown in Figure ???.

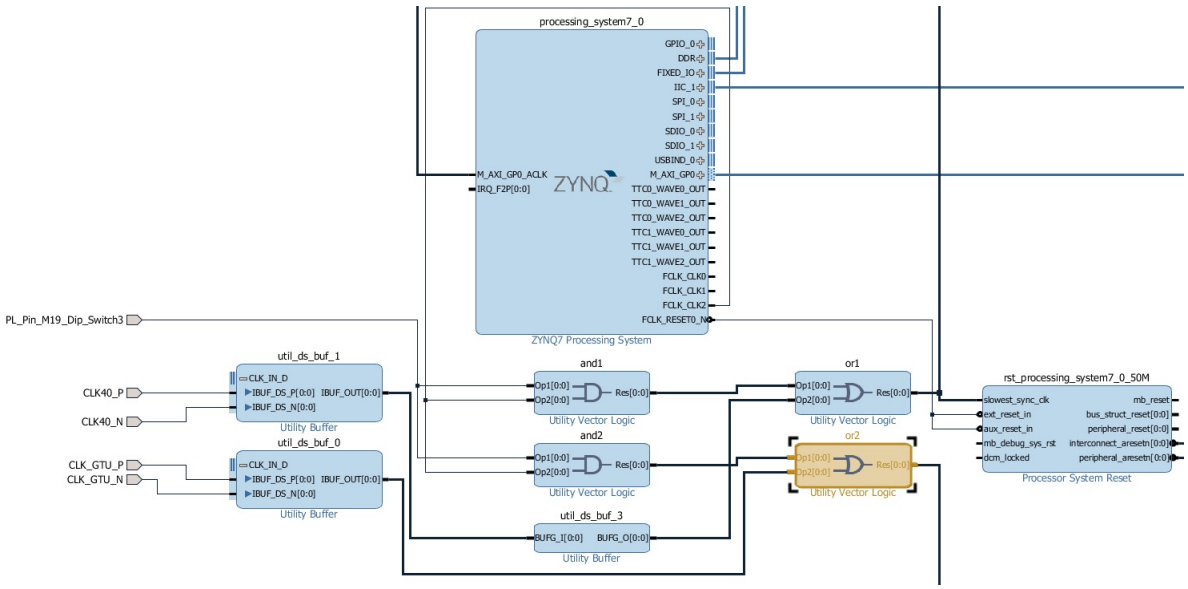


Figure 47 – The clocking logic of the VHDL design shown at the graphical top level. The LVDS input ports of the system clock (CLK40_P and CLK40_N) and the GTU clock (CLK_GTU_P and CLK_GTU_N) on the left are routed to the LVDS buffers and to the switching logic from there. The Dip_Switch3 is responsible for switching clock modes from external to internal, while the internal fabric clock is routed from FCLK_CLK2 of the processing system block.

5.7.3 Data transaction from the PS and buffering

The internal connection between PS and PL is established via an AXI4 general purpose port as already mentioned in Section ???. The Vivado framework provides an IP-Core solution called AXI4 peripheral, which manages the data handling of the bus and provides up to 512 slave registers for reading and writing commands. In this case 16 registers have been proven to be sufficient as there is no need to transfer the data packages parallel via several ports. Each register has a 32 bit width and has its own RAM address on the PS side. Within the wrapper module of the AXI4 peripheral the interface logic for fetching the data from the slave registers has been implemented. Figure ??? shows the flow chart of the main transaction state machine. When the PL has booted the process starts with resetting the six data FIFOs and then switches into idle state after two clock cycles. In the idle state the process checks for the data ready signal from one of the AXI4 slave registers and switches into receive state if the signal has been asserted. The receive state reads out the 8 bit data package and stores it into the first of six FIFOs which correspond to the six MAPMTs connected to the original SPACIROC. The process then switches back to idle, waiting for the next package.
As the data transaction from the UART interface is done with a rate of 115200 Bit/s which is comparatively slow to the 40 MHz clocking of the state machine, the process will remain in the idle state for most of the time. After 64 data packages are received, the next package belonging to another MAPMT is stored into a different FIFO. The process repeats itself and starts filling the first FIFO again after the data of six MAPMTs has been received.
When the complete test data frame has been sent the PS asserts a transaction finished signal at one AXI4 slave register, which is processed in the idle state and triggers the switching to the send state. If the transmit signal is asserted from the PDM, the process waits for a rising edge of the GTU clock to read out all six FIFOs simultaneously. One clock cycle later the process has to prepare the data for sending to the PDM according to the parallel bus protocol of the SPACIROC. This part of the program will be described in depth in the next Section.

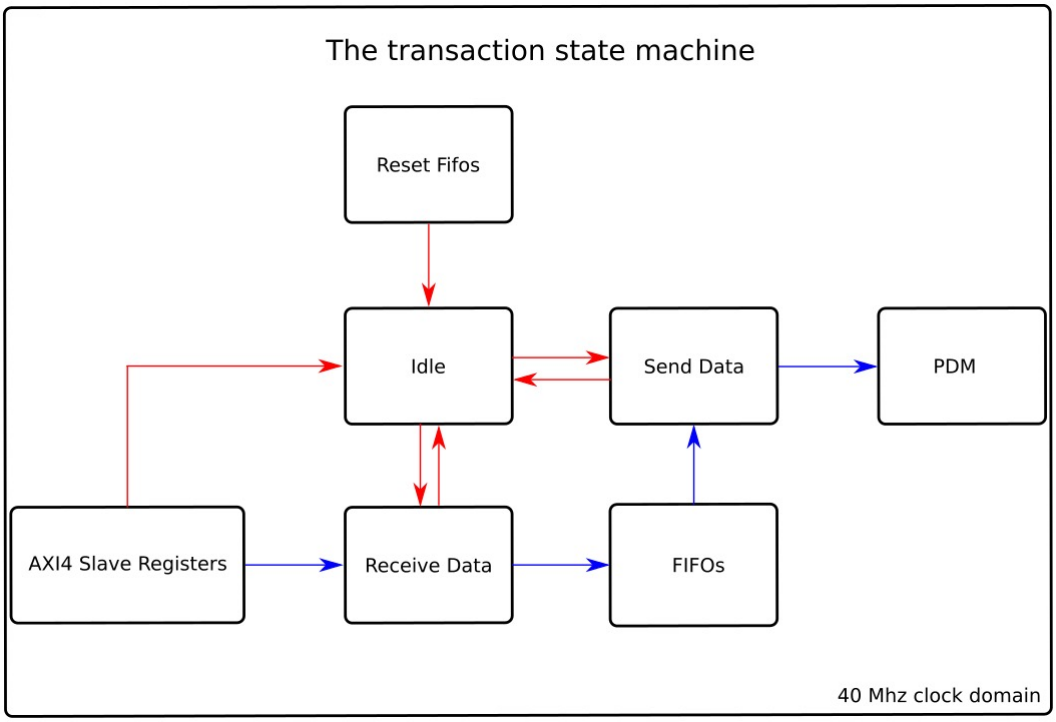


Figure 48 – The schematic of the transaction state machine. The control signals are drawn in red and the data signals are drawn in blue. The process is implemented in the 40 MHz system clock domain.

5.7.4 The parallel interface to the PDM

The interface of the SPACIROC to the PDM consists of six parallel 8 bit channels resulting in 48 single pin connections. In every GTU cycle eight data packages are transmitted per connection, which corresponds to the 64 packages for one MAPMT and one channel. The transaction protocol starts with a start bit followed by the 64 bit of the eight packages and ends with a parity bit. The packages are always transmitted with the Most Significant Bit (MSB) first and there are no idle clock cycles between the single packages. Originally a separate TransmitOn signal was planned to be asserted during one transaction cycle, but was removed in later versions of the SPACIROC as its function was proven to be redundant and the reserved IO could be saved. Figure ??? shows the old and the new version of the protocol structure.

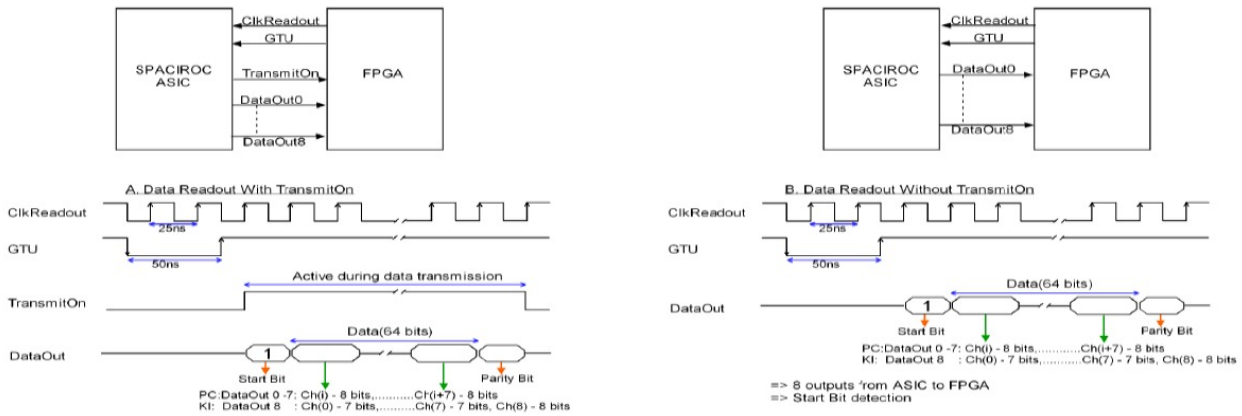


Figure 49 – The TransmitOn controlled readout system is shown on the left. The Start Bit controlled readout system is shown on the right. The current implementation uses the Start bit readout system. Image: [28]

When the state machine has switched to the send state and a rising edge of the GTU clock has been detected, the process starts with calculating the parity bit for the protocol. The data read out from the FIFOs have to be transformed into the correct order before they can be sent to the 48 output buffers of the parallel bus. The first step is to reverse the order of every 8 bit data package, which is required as the transaction of one package always starts with the MSB. Additionally, the 64 data packages have to be distributed onto the eight channels. This is achieved by storing eight data packages for each channel into a register array which is connected to the output ports. The operation is done in a finite for-loop counting up the number of FIFOs. In contrast to classical for loop structures in different programming languages, for loops in VHDL are able to perform their operation fully parallel and within one clock cycle, but can potentially use a big part of the logic resources, as every loop iteration has to be mapped on the PL individually. In this case though the hardware resources are sufficient and the for loop has only six iterations.
After 64 clock cycles the transaction of the information payload has ended and the parity bit is sent before the state machine either repeats the sending operation for the next GTU cycle or switches back to idle if the FIFOs are emptied.

5.7.5 Control and debug functions

In this section the assignment and functionality of the switches and LEDs of the ASB, as well as the utilization of the PL debug cores will be described. The eight switches of the board are utilized for different core features of the PL functionality.
Table ??? gives an overview of all switching states. Switch 1 switches between PS and PL transaction and a separate VHDL module which generates random grey encoded data packages. This function was proven to be useful in the early stages of the development, as the output ports could be tested easily, without any programming of the PS.
Switch 2 is used as a soft asynchronous reset for the VHDL module responsible for the data handling and transaction.
Switch 3 selects the clock source between internal and external clock (see Figure ???).
Switch 4, 5, 6 and 7 are utilized as multiplexers for generating a fixed 8 bit number for all output ports of the PDM bus. This feature allows to debug single malfunctioning output ports quickly as the values stay constant and can also be measured with an oscilloscope or multimeter.
Switch 8 is unused in the current design.

Table 4 – The function of the 8 hardware switches

Switch number	State	Function
Switch 1	0	PS to PL transaction mode
	1	PL random package generator
Switch 2	0	soft reset
	1	normal mode
Switch 3	0	internal system clock
	1	external system clock
Switch 4, 5, 6, 7	0 - 15	fixed number for PDM bus output ports
Switch 8	—	not used in design

The LEDs of the ASB are mainly used to display different states of the PL design for internal debugging and have been changed constantly during the development phase of the

VHDL design. Therefore, only the function of LED 7 and 8 are listed here as the others are subject to change and would likely not fit any description given in this thesis.
LED 7 and 8 are connected directly to the System Controller (SC) IP block and display the state of the SoC. LED 7 displays the presence of the 3.3 V supply of the micro module, while LED 8 indicates that the SoC has booted. All LEDs can be wired to different signals any time if there is a need for it in an updated design.
In addition to the LEDs a Virtual I/O (VIO) debug core has been included in the VHDL design, which is utilized for displaying the state of various signals. This core also supports the usage of virtual outputs as "software switches", but this functionality was not used in the latest design. Similar to the LEDs the assignment of the monitored signals has been changed several times so there will be no list of signal assignments given.
The final and most important debug function of the current design is the Internal Logic Analyser (ILA) debug core, which integrates the former ChipScope debugger into the graphical Vivado environment. As already mentioned in Section ??? it monitors different signals and shows their state in a testbench using the XILINX ISIM tool. Table ??? shows the signal assignment of the current design.

Table 5 – The signals monitored by the ILA core

Channel	Signal	Bit width
1	MAPMT A output	8
2	Data KI output	6
3	FIFO debug vector	8
4	State indication vector	4
5	MAPMT B output	8
6	MAPMT C output	8
7	MAPMT D output	8
8	MAPMT E output	8
9	MAPMT F output	8
10	GTU clock	1

5.8 The ASB adapter board

Besides its main task, the ASIC-Simulation Board also has the ability to be utilized in a variety of project unrelated applications, as it provides several data interfaces and sufficient debug functionality (see Section ??? and ???). New students at the IAAT will use it as development platform for small projects, which will introduce them to the SoC technology. For this reason an additional adapter board has been designed which is connected to the 120 Pin connector of the ASB and enables the free usage of 64 additional I/Os.
The circuit diagram of the adapter board is shown in Figure ???. The 120 Pin connector at the left (X7) will be plugged on the ASB, while the two 32 Pin connectors (K1 and K2) on the right provide an easy access to the I/Os. The board is powered with 12 V and its power connector (J1) is located at the top left. Two linear power supplies on the top of the board provide either LMZ12008 (X1) or 5 V (X5) supply voltage for the I/O Pins and have eight connection pins each (K3 and K4) for external power supply. A single connector with eight ground pins (K6) has been implemented as well at the right bottom side of the board.
Eight levelshifters (X3 and X8-X16) along the middle of the board are necessary to transform the logic level of the signals from 3.3 V or 5 V to the 1.5 V LVCMOS standard of the corresponding

ZYNQ I/O-banks. The logic level can be switched by two jumpers (J2 and J4) in the center of the board, allowing to operate each four levelshifter with different logic voltages. The 64 I/Os have to be used as single ended signal, but the adapter board additionally provides three LVDS I/Os on a separate connector (K5) at the bottom left.

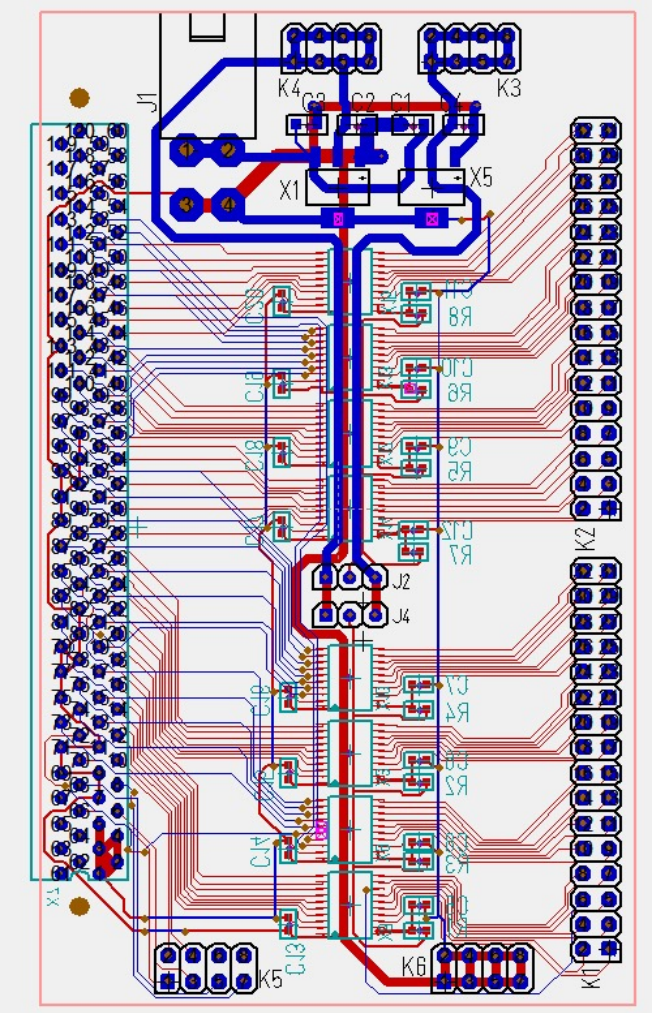


Figure 50 – The circuit design of the ASB adapter board. The board has two copper layers located at the front and the back. The blue signals refer to the front layer, while the red signal are routed on the back layer. The front layer is mainly used for power signal routing and connecting some signals from the 120 Pin connector to the levelshifters, while the back layer routing includes most of the signal routing and the ground distribution.

6 Test Setup and Results

6.1 Overview

In preparation for the EUSO-SPB flight in April 2017 the original plan was to implement the updated First Level Trigger (FLT) algorithm till January 2016 and test its functionality on the updated Photo-Detector Module hardware with the help of the ASIC-Simulation Board until July 2016. The PDM then had to undergo a series of thermal tests in August 2016 at the Colorado School of Mines, USA. While the trigger implementation was successfully completed to the end of 2015, the circuit design and manufacturing of the ASB was not finished till June 2016. From May 2016 there was already an original SPACIROC3 board available at the IAAT,

which allowed the execution of all required testing steps of the FLT leading to the thermal tests. The function tests of the FLT where repeated with the use of the ASB instead of the original hardware in January 2017.
During the commission of the ASB carrier board several hardware tests were performed to ensure good signal quality and a stable power supply, which are described in Section ???. The details of the integrated test setup with the ASB connected to the PDM and its results are given in Section ???.

6.2 Test of the ASB hardware

The first step of the carrier board commissioning was to ensure that there are no short-circuits between the different power connections and the ground network. This was followed up by testing all signals for correct connectivity at which point the bridge between two LVDS signals of the Ethernet interface was detected (see Section ???).
For the power supply two different tests were performed. The first test checked the function of the under- and over voltage protection as well as the short-circuit protection of the LMZ12008 step down power module before the micro module was connected to the carrier board. The LMZ12008 switched the 3.3 V power off immediately when a short-circuit was applied. The threshold for under voltage shut down was found at 5.0 V and for over voltage shut down at 20.2 V. Between these two threshold values the output voltage remains constant at 3.27 V, which is an acceptable result considering that all devices operating on the carrier board have at least an input voltage tolerance of ±5 %.
The second test measured the input current and therefore the power consumption for the final hardware implementation for different input voltages. Starting from the lower input threshold of 5.0 V the current was measured in 0.5 V steps till 15 V. Despite the successful tests of the over voltage protection it was decided to not risk any damage of the hardware and therefore not exceed 15 V. The table ??? shows the measurement results and the calculated power consumption of the ASB.

Table 6 – The input voltage and current with the calculated power consumption

Input voltage	Input current	Power consumption
5.0 V	0.45 A	2.25 W
6.0 V	0.37 A	2.22 W
7.0 V	0.32 A	2.24 W
8.0 V	0.29 A	2.32 W
9.0 V	0.26 A	2.34 W
10.0 V	0.24 A	2.40 W
11.0 V	0.22 A	2.42 W
12.0 V	0.20 A	2.40 W
13.0 V	0.19 A	2.47 W
14.0 V	0.18 A	2.52 W
15.0 V	0.17 A	2.55 W

The measurement results show a slight increase of power consumption for higher input voltages, which fits to the decreased efficiency of the LMZ12008 for higher input voltages, especially at low output currents [59]. The expected power consumption of 1.74 W of the

ZYNQ SoC for the final implementation also seems to fit to the average power consumption of 2.38 W, as the LMZ12008 effiency is expected to be $\sim 80\,\%$ at 12.0 V and 0.20 A [59] and there are no other major consumers.

6.3 Test setup at the Institut für Astronomie und Astrophysik Tübingen (IAAT)

Figure ??? is the schematic of the test setup with all involved hardware, while Figure ??? shows the laboratory setup at the IAAT. The PDM and the CCB are powered by a sensitive laboratory power supply which allows to control the output voltage within a 10 mV precision. A second commercial power supply is placed on top and provides the 12 V power for the ASB. The ASB itself is plugged onto the PDM and connected to a host computer via the UART interface (the white mini USB cable) and the JTAG interface (the flat USB-JTAG programming cable). A customized shielded LVDS cable connects the PDM to the CCB and the yellow Spacewire cable establishes the connection to the computer on the left. The computer replaces the real CPU of the Mission Data Processor and also directly observed the First Level Trigger and data signals of the PDM via Chipscope for debugging purposes. The test data was extracted from a data bundle of EUSO Balloon mission and included several frames with photon tracks induced by laser shots, which were performed during the mission. The testing procedure of the FLT is explained in the next section.

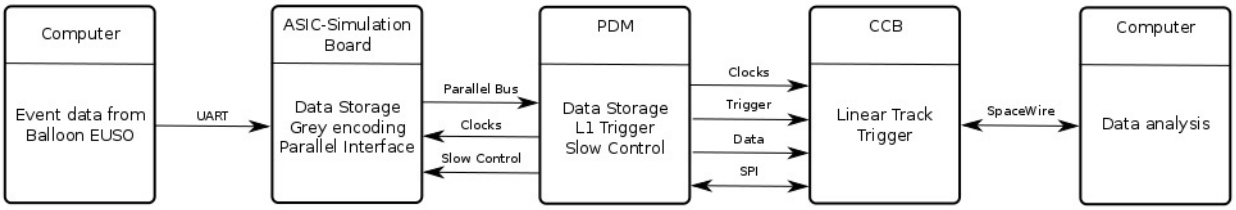


Figure 51 – Schematic of the hardware test setup: The test data provided from the EUSO Balloon mission is sent from a computer to the ASIC-Simulation Board. From there the data is grey encoded and sent to the PDM. If a L1 Trigger is issued the data is sent to the CCB, which performs the Linear Track Trigger and sends the triggered data back to the computer. The system clock and the GTU clock are generated at the PDM.

6.4 Test of the First Level Trigger

The updated First level Trigger implementations (Version 6.5D-1 to 6.5D-3, see Section ???) have first been tested on several hardware simulation testbenches. The Xilinx ISE design suite provides an internal testbench tool called ISim, which simulates the behaviour of VHDL modules and can be configured to read out test data from external documents and use it for the simulation.
The test data package originates from the FLT implementation of previous versions and consists 25300 frames of one EC including several trigger events. The data is organized in 8×8 photon counts representing one MAPMT each, and therefore allows simple manipulations of single 3×3 trigger boxes.
When the simulation starts the data gets written to the input ports of the FLT VHDL top module, while internal signals as well as the trigger outputs are displayed at the testbench GUI for every system clock cycle. The different threshold values can be freely configured and the

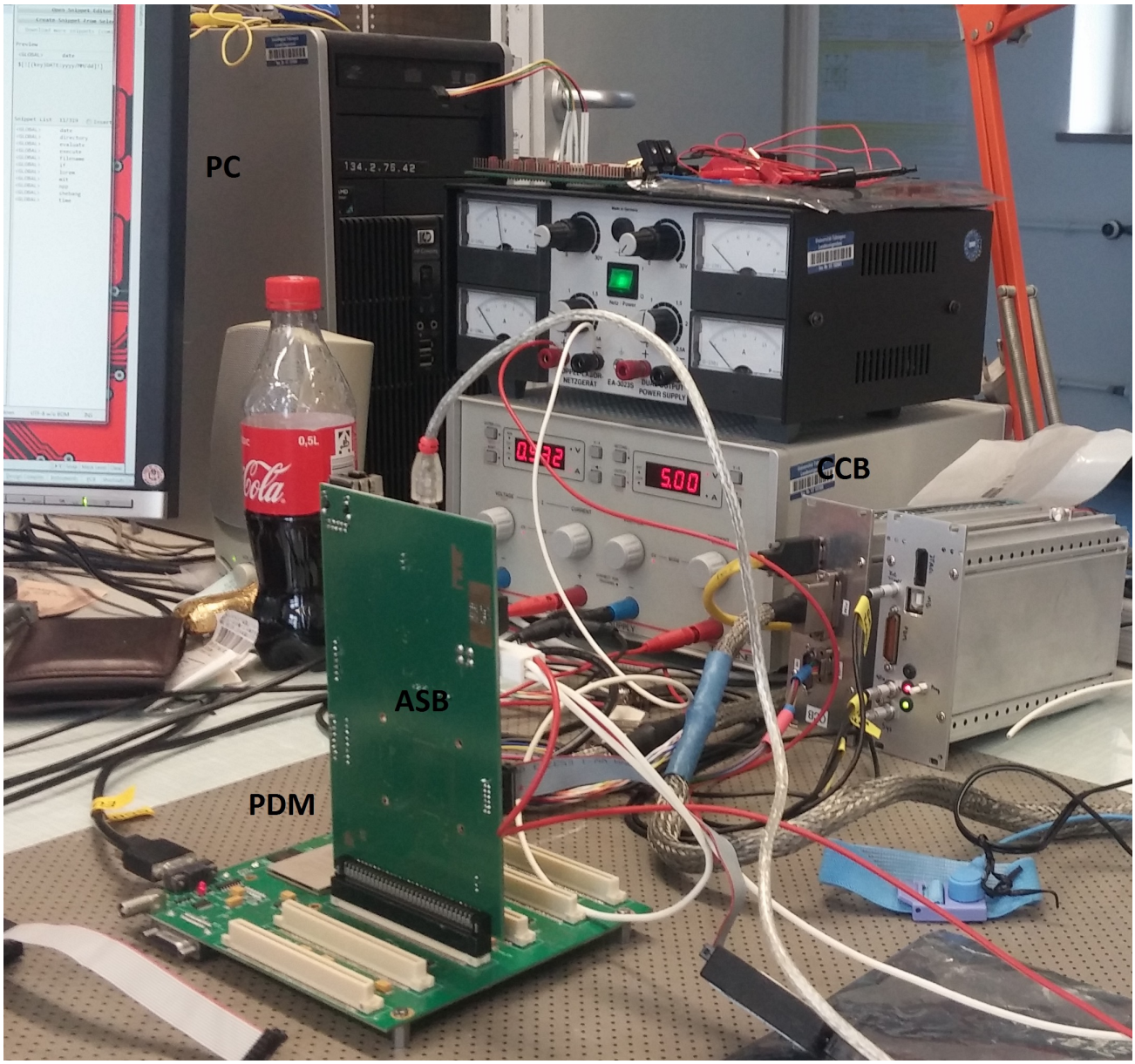


Figure 52 – Picture of the setup at the IAAT laboratories: The ASIC-Simulation Board is plugged onto one of the six 120 pin connector of the PDM (lower left). The CCB (middle right) is connected to the PDM via a shielded customized cable, and to the PC (upper left) via the yellow SpaceWire cable. The white power supply (center) provides power for the PDM and CCB, while the black power supply on top provides the 12 V power for the ASB. The test data is transmitted to the ASB via the white USB cable (center).

auto threshold calculation can be switched off.
Every trigger event is written into a data file at the end of the simulation, containing the GTU number starting from zero, the vertical and horizontal position and the total photon count of the corresponding 3×3 box.
For every version of the trigger implementation the simulation was performed four times with the preset threshold values (see Section ???). In the first run the auto threshold calculation was activated, while for run two to four the the N threshold (amount of photons per pixel) and S threshold (amount of photons per 3×3 box) were set to the values shown in table ???.

Table 7 – The selection of N and S thresholds for the trigger simulation

Test run	N threshold	S threshold
1	auto	auto
2	2	5
3	5	35
4	9	60

For test run one, three and four the resulting trigger events matched exactly the events detected by the original implementation, while for test run two additional trigger events were written into the output data file. After several days of testing and communicating with Marcio Mignone and Mario Bertaina from the University of Torino it appeared the high amount of trigger events occurring for low manual threshold settings causing the FIFO responsible for storing the pretrigger events to overflow in the original design. In the updated implementation the FIFO belongs to the 80 MHz clock domain so events are read out with double speed compared to the original code and the overflow is prevented that way.
This issue also showed the importance of the auto threshold calculation for the background, as otherwise the trigger rate might reach levels which exceed the mission's data budget by far.

After the successful simulation test runs the FLT a series of test runs were planned with the hardware setup, described in Section ??? for January 2017. One major problem of the hardware testing was the small time window in which the tests had to be completed. One of the two updated PDM boards, which had been manufactured for the EUSO-SPB mission had already been integrated in the instrument in middle of 2016, while the second one had to be shipped to Wanaka, New Zealand on the 10th of February 2017 to serve as spare board in case of technical problems. Additionally the customized cable between PDM and CCB was inoperable and had to be repaired, which shrunk down the available time for testing to six days. At that time is was expected to receive the PDM spare board back within late April 2017, which would have allowed to rebuild the setup and continue testing before the deadline of this thesis. The launch of EUSO-SPB was postponed several times until April 24th and the spare board will not arrive at the IAAT before middle of June 2017. Due to these circumstances one of the major goals of the test runs, to use the data provided from EUSO Balloon for tests of the complete trigger chain from the ASB up to the Mission Data processor was not achieved.
As a first step the system clock and the GTU clock provided by the PDM were monitored with the Integrated Logic Analyser (ILA) (see Section ???) at Programmable Logic level of the ZYNQ SoC and then switched from internal to external (see Section ???). The next step was to send an identifiable bit-pattern via the a port of the parallel bus interface to check the bit mapping of each channel. For that the data received by the PDM and stored in its ring buffer was monitored with Chipscope via the JTAG debug interface simultaneously and compared to

the original bit pattern. After several problems with the mapping order of the data, the grey encoding and the parity calculations had been solved the testing was continued for all other channels of the parallel bus.
After the correct bit mapping was ensured for every single channel and the global reset from the PDM was tested, the same test data used for the FLT simulations was sent to the ASB in order to cross check the amount and position of trigger events with the results of the simulations. Several trigger events were detected via the SpaceWire interface from the CCB and also directly by Chipscope with was configured to surveil the internal trigger signals of the PDM, but the events did not fit to the trigger events from the simulation results. At first there was no explanation for this result, as the data transmitted by the ASB seemed to be correct and the FLT was already tested several times on PDM level with the original SPACIROC3 hardware. After a number of tests it was shown that a timing problem persists between the ASB and PDM, resulting in some bits of the parallel bus being sampled on the wrong flank of the system clock. The VDHL code on both sides was checked several times but the problem could not be found on time, as the PDM board was only available until 10th of February 2017. Despite this problem the tests showed that the ASB is able to process test data according to the parallel bus protocol, and that all signals between ASB and PDM are connected correctly and are working properly. The reason for the wrong bit sampling should be explored in the future to allow use of the ASB for further testing with the new data collected from the EUSO-SPB mission.

7 Conclusion & Outlook

The implementation of the updated First Level Trigger for the Photo-Detector Module constitutes as the first part of this master thesis. Its final version meets all area and timing constraints of the PDM FPGA, while maintaining the necessary functionality which as been tested in simulations as well as on the original hardware. It became part of the final VHDL implementation for EUSO-SPB instrument and performed well during the eleven day flight duration of the mission. The amount of logic that was saved with the updated Trigger version will allow to implement additional features on the PDM FPGA in the future.
The second part of this thesis was the development, manufacturing, programming and testing of the ASIC-Simulation Board to be used in laboratory and field tests of the focal surface electronics of the EUSO-SPB mission. The current version can be utilized as a replacement for the original ASIC board to feed the PDM with free configurable data. This is an important point as the IAAT is responsible for further developments of the PDM Board since 2015. In comparison to the original hardware, for which a pulse generator has to provide a test signal for the SPACIROC3, the ASB allows to send complete sequences of either simulated or real data from past missions to the PDM. This makes testing of further developed versions of the PDM and the complete data processing of the focal surface electronics up to the Mission Data Processor significantly easier. Besides the timing problem occurring wit some bits during the transaction between the ASB and PDM, the board is fully functional.
The ASB is also the first hardware project of the IAAT, that employs a Xilinx ZYNQ SoC instead of a common FPGA. This relatively new architecture of a combined processing system and FPGA structure was chosen on purpose, to not only introduce this new technology to the institute but also enable students, which are interested in embedded systems to use the ASB as a development board for future hardware projects. For that reason an additional adapter board was designed, which allows 64 I/Os originally designated to the parallel interface between ASB and PDM to be used freely with either the 3.3 V or the 5 V standard.
After the successful launch of EUSO-SPB a new super pressure flight with the EUSO instruments has already be announced and is called EUSO-SPB 2, but it is currently unclear if the development of the focal surface electronics will proceed at the IAAT or being shifted to the participating institutes in the USA. If however the project will be continued at the IAAT, the first goal would be to fix the above mentioned synchronisation problem of the interface between ASB and PDM.
A further development of the ASB would include to use the external RAM for long term storage of different test data packages which could be selected by the onboard switches of the ASB. This would allow its usage for several test scenarios with complete independence from a computer.
The unique architecture of the ZYNQ SoC together with the adapter board also allows the ASB to be deployed for applications in which a large amount of data has to be sampled fast and stored before being processed by a Linux operation system within the SoC. In August 2016 Xilinx introduced a tool that allows the developed to describe the complete hardware functionality in C code instead of VHDL for the Programmable Logic. The tool then would decide by itself which functions could be shifted to the hardware level and implement the whole system during one compiler run. Exploring the feasibility of this work flow might also be of interest, as it enables software developers to program hardware to a sufficient level without deep knowledge of VDHL and FPGA design.
In summary this master thesis will have fulfilled its complete purpose when there is proof that the first ultra high energy cosmic ray has been detected by the EUSO instrument.

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List of Acronyms

Declaration

I declare that I have developed and written the enclosed master thesis completely by myself, and have not used sources or means without declaration in the text. Any thoughts from others or literal quotations are clearly marked. The master thesis is not used in the same or in a similar version to achieve an academic grading or is being published elsewhere.

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