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Note from the IBIS PI Team on the Scientific Data Processing for the INTEGRAL/IMAGER

Scientific Processor Unit (**SPU**) / Digital Processing Electronics (**DPE**)

1. Summary

This document is a summary of the situation on the scientific data processing as it has evolved and as it has been agreed upon by all groups involved during the recent meeting in Saclay on 28 November 1995.

Reference documents are:

general: EID-A and EID-B

from Tübingen:	IN-IM-TUB-TN/EL-001, Issue 1, 02.08.1995 IN-IM-TUB-TN/EL-002, Issue 1, 11.09.1995 IN-IM-TUB-TN/EL-003, Issue 1, 05.09.1995 IN-IM-TUB-TN/EL-004, Issue 1, 20.11.1995 IN-IM-TUB-RP/EL-001, Issue 1, 05.09.1995
from Saclay:	IN-Im-Sap-RP-0016 (P. Laurent, Background Evaluation for the New Imager, 07/95, P. Laurent, e-mail to R. Staubert on 27.07.95 IN-IM-SAP-RP-0009, Issue 4, 31.07.1995 SAP-ISGRI-PI-0222-95, 24.11.1995
from Bologna:	IN-IM-TES-RP-0006, 24.11.1995
from ESTEC:	PG/10.3.2/500/rt, 20.11.1995

Minutes of the meeting in Saclay on 28 November 1995.

The following points are the essential conclusions:

1) The high event rates, particularly from the CsI layer, require an additional electronics unit (the Scientific Processor Unit - SPU) between the layer electronics and the Data Processing Electronics (DPE).
2) The SPU must be a hardware processor, again because of the high event rates.
3) The event data will be delivered by the layer electronics in digital form. The events will be ordered in time by each layer.
4) The SPU will be a hardware processor which will identify time coincidences between events in the CdTe and the CsI layers and will store CsI detector images in different energy intervals.
5) The SPU will be realised as one additional electronics board which will be accomodated in the DPE box.

2. General considerations

The information about events in the detetors of the IMAGER (CdTe array, CsI array, BGO veto and Calibration source detector) is digitised in the Module Controle Electronics (MCE), channeled through the Scientific Processor Unit (SPU) to the Digital Processing Electronics (DPE) and finally handed over to the Onbord Data Handling System (OBDH) for telemtry.

We make the following baseline assumptions about the SPU/DPE:

A) The SPU/DPE must be able (under the constraints given) to satisfy the needs for a near optimum scientific exploitation of the information produced by the IMAGER detectors.
B) The SPU should be as simple as possible (without compromising the science) in order to reduce development cost.
C) Full use is to be made of the capabilities of the DPE provided by ESA.
D) The number of events (amount of information) to be handed over to the SPU should be reduced to 'useful' events (information) as much as possible.
E) Because of the high event rate in the CsI (order 20000 cts/s) it will not be possible to transmit the full information event by event. Instead, detector images will be accumulated.

Under the above assumptions the following general scheme is foreseen:

1) The Module Control Electronics (MCE) should apply analog anticoindence information as much as possible in order to throw out 'obvious' background events in CsI and in CdTe before input to the SPU. Where this is not feasible (CdTe-ASICS?), the possibility for introducing coincidence flags (CdTe/BGO, CdTe/CsI) should be considered in order to ease the task of the SPU.

2) The SPU should be realised by hardware, that is without processor, but with programmable parameters to be set by the DPE. This 'hardware filter' has the task of further reducing the number of events (amount of information) which is to be handed over to the DPE. The two main tasks are: identification of coincidences/anticoincidences and applying a 'Compton logic' for those events coincident in CdTe/CsI - in order to throw out 'bad' events. The number of 'bad' events will be counted and recorded. The 'good' events will be passed to the DPE. The SPU will be a slave to the DPE. Commands will be channeled from the DPE through the SPU to the MCEs.

3) The DPE will perform the following functions:

- support various operating modes
- provide command interface between OBDH and the instruments
- receive event information from the SPU
- apply further cleaning and/or data reduction
- produce detector images for the CsI events
- accumulate energy spectra
- distribute clock signals
- collect housekeeping information from the instruments and feed into telemetry
- apply compression where applicable
- perform 'packatising' for the ESA telemetry
- hand all data over to the OBDH for telemetry

Under the assumption that the basic telemetry capacity allocated to the IMAGER will be about 40 kbit/s the majority of the CdTe-only events can be transmitted in an event-by-event mode. This may also be possible for the Compton (CdTe/CsI) events if the SPU can indeed provide a reduction in rate (select those events from the proper FOV). The CsI events will have to be accumulated as 'detector images' in a number (e.g. 128) of energy channels and over a certain integration time (e.g. 1000 s). The DPE (as currently defined: max. input rate 1Mbit/s, memory 2 Mbyte, computing power 1.5 Mips) should be able to fulfil the above tasks.

4) The DPE/SPU should allow the operation of a 'Transparent Mode' by which 'primary' information from the detectors (not vetoed, not screened or cleaned) may be transmitted. This is to be used for diagnostic purposes.

3. Event Types and bits per event

The CdTe detector has 128 x 128 = 16384 = 10^{14} elements.
The CsI detector has 64 x 64 = 4096 = 10^{12} elements.

Event types are refered to according to EID-B, Section 1.7.1. For the allocation of bits per event we make use of information given in the minutes of the Frascati meeting of 09.03.95. For relative timing 14 bits per event are assumed (this allows an accuracy of somewhat better than 0.1 ms, if a reset occures every second).

Table 1

Event Type	Description	amplit.	rise time	position	timing	total
0	CdTe only <50 keV	10	0	14	14	38
1	CdTe only >50 keV	10	7	14	14	45
2	CdTe/CsI: CdTe	10	7	14	14	45
2	CdTe/CsI: CsI	9	0	12	0	21
3	CsI	9	0	12	14	35
4	BGO	9	0	0	14	23

4. Event rates and data flow

4.1. Expected event rates

For the expected event rates we refer to values given in IN-IM-SAP-RP-009, Issue 4.

For our calculation we have taken the maximum values and made the following simplifications. The rate from one CdTe module is 300 events/sec and he primary event rate per module in CsI is a factor of 7 higher. This leads to event rates from the detectors:

- CdTe: 2400 events/s
- CsJ: 27720 events/s (The primary event rate of 16800 events/s is increased by a factor of 1.65 due to multiple events.)

4.2. Data Processing Tasks

Figure 1 shows the data flow from the detectors to the SPU/DPE and indicates in round boxes the data processing tasks necessary to cope with the limited telemetry capacity asigned to IBIS.

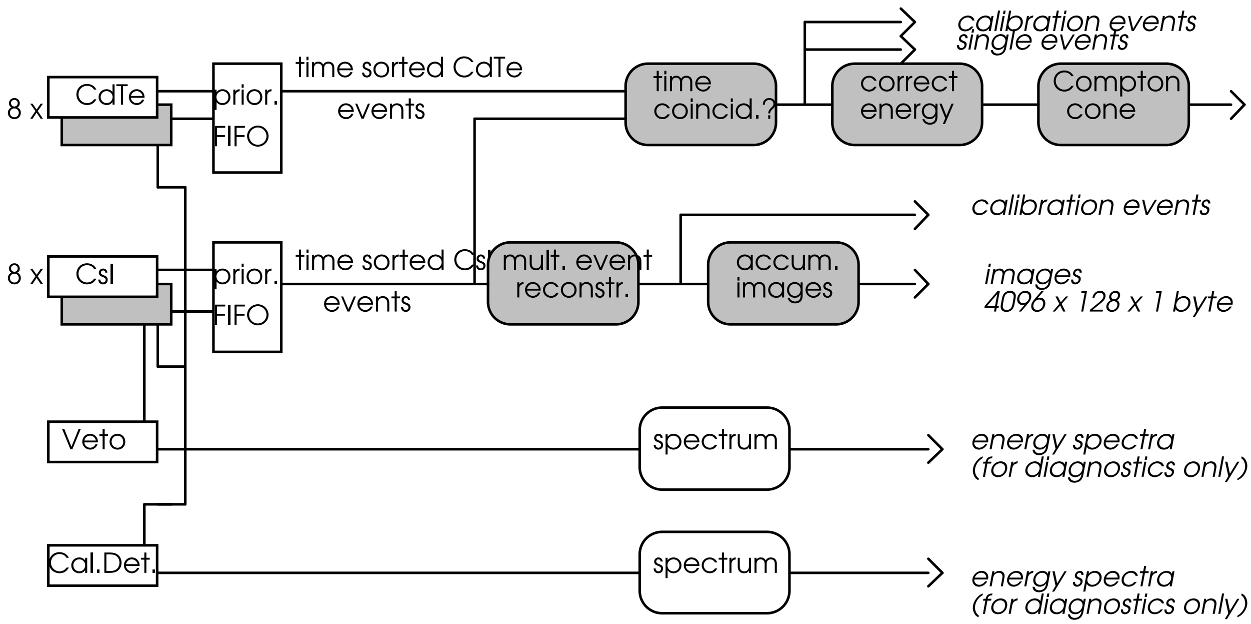

Figure 1. Data flow in DPE, filled round boxes indicate major processing tasks

4.3. Processing Load

We have tried to estimate the processing load for the different tasks indicated in Figure 1. Energy spectra from veto detectors and from the calibration detector will only be accumulated for diagnostic purposes. These tasks do not contribute to the processing load during normal operation. Therefore these two tasks are not further considered.

In order to estimate the processing power needed, we have written the algorithms in C language. The code then was compiled by an 68000 cross compiler and the number of assembler instructions counted. A 1750-type microprocessor (not 68000) will be used and the high level language used will be ADA (not C) therefore the results can only be taken as a first order estimate.
A more detailed analysis of the processing load is given by Martin Mohan in his report IN-IM-TUB-RP/EL-001.

Table 2: Computing load for DPE

Description of task	instructions/ event	events/s	computing load in MIPS
search event data for time coincidences CdTe- CsI	184	2400	0.44
correct energy of Compton CdTe events	40 [1)]	1200	0.05
compute Compton cone for CsI/CdTe events	80 [1)]	1200	0.10
accumulate CsI images, including handling of multiple events	44	27720	1.22
miscellanenous	40 [1)]	2400	0.10
subtotal of scientific processing			*1.91*
handling of OBDH interfaces (CMDs and data packetizing)			0.20
total processing load	-	-	2.11

Remarks:

1): Only very preliminary assumption, real algorithm not yet defined. We propose to use look-up tables in order to reduce computing time, if necessary.

The required total processing load is much higher than the available processing capability of the baseline DPE which is of the order of 1.4 MIPs. The situation becomes even worse, if one applies margins to these figures as required by the INTEGRAL Software Requirement Document (SRD). Margins of 1.33 and 2.0 are required during phase B for scientific processing and for data management tasks, respectively. Including those margins a computing capability of the DPE of 2.95 MIPs would be required, which is a factor of 2.1 above the current baseline, so we have a severe problem.

After discussion with the project a solution to solve the problem was found. This is described in some detail below.

5. Proposal for a Hardware Event Preprocessor for IBIS (HEPI)

A "Hardware Event Preprocessor" (HEPI) could perform the following tasks:

- collect event data from CdTe and CsI detectors (It is assumed that the events are sorted in time by layer.)
- search event data for time coincidences CdTe - CsI
- reconstruct multiple CsI events
- accumulate CsI images for fraction of energy range
- send event data and accumulated images to DPE
- *distribute time clock and time synch to all MCEs.*

If all multiple CsI events would be reconstructed by hardware and if for 50% of all CsI events HEPI would accumulate images, we could significantly reduce the computing load for the DPE from 2.11 MIPs to 0.82 MIPs (*1.22 MIPs including margins*), see Tab. 3.

Table 3: Computing load for DPE processor with a hardware preprocessor

Description of task	instructions/ event	events/s	computing load in MIPS
search event data for time coincidences CdTe- CsI	184	2400	N.A.
correct energy of Compton CdTe events	40 [1)]	1200	0.05
compute Compton cone for CsI/CdTe events	80 [1)]	1200	0.10
accumulate CsI images for 50% of events **excluding** handling of multiple events	44	8400	0.37
miscellanenous	40 [1)]	2400	0.10
(subtotal of scientific processing			*0.62)*
handling of OBDH interfaces (CMDs and data packetizing)			0.20
total processing load	-	-	0.82

All the required hardware could be built on one board (>100 x 160mm^2), and would consume 2-3 Watts @ 5V (TBC). All connections to the DPE would only be via standard fast and slow serial interfaces, i.e. HEPI would have no direct access to the DPE bus.
In order to keep interfaces clean and to simplify AIV activities, this board should be housed inside the DPE box and should be powered from the DPE.

Figure 2 shows a simplified block diagram of HEPI.
Event data from the detectors are read via serial interfaces to the preprocessor. After flagging time coincident events and further processing (reconstruction of multiple CsI events, accumulation of images), data are written to DPE via the two standard high bit rate interfaces. The preprocessor can be commanded through a standard low bit rate interface. This interface is also used to send HK information (status of HEPI) to the DPE.

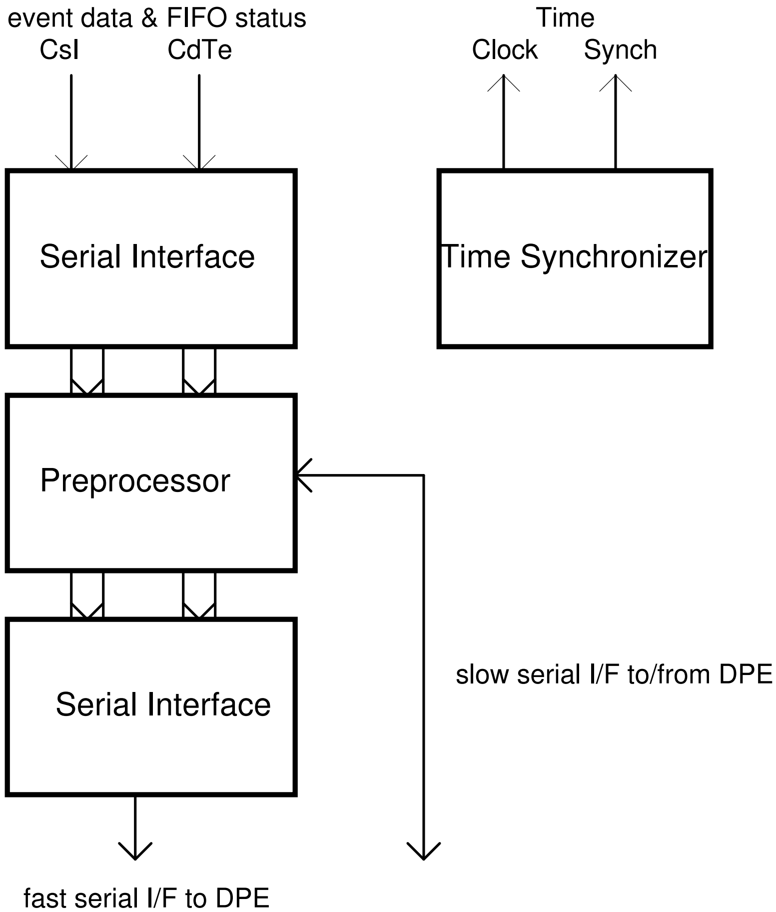

Figure 2: Block diagram of HEPI

In Figure 3 the functional blocks of the preprocessor are shown. The functioning of HEPI is controlled by registers, which are set through the slow serial interface. Data are read from the detectors and times are searched for coincidences. CdTe events which coincide with CsI events are flagged before they are written to an output FIFO. CsI events with energies within a selectable range are accumulated to event maps in an 512 kbyte RAM (TBC). The content of this RAM can be dumped to DPE on command.

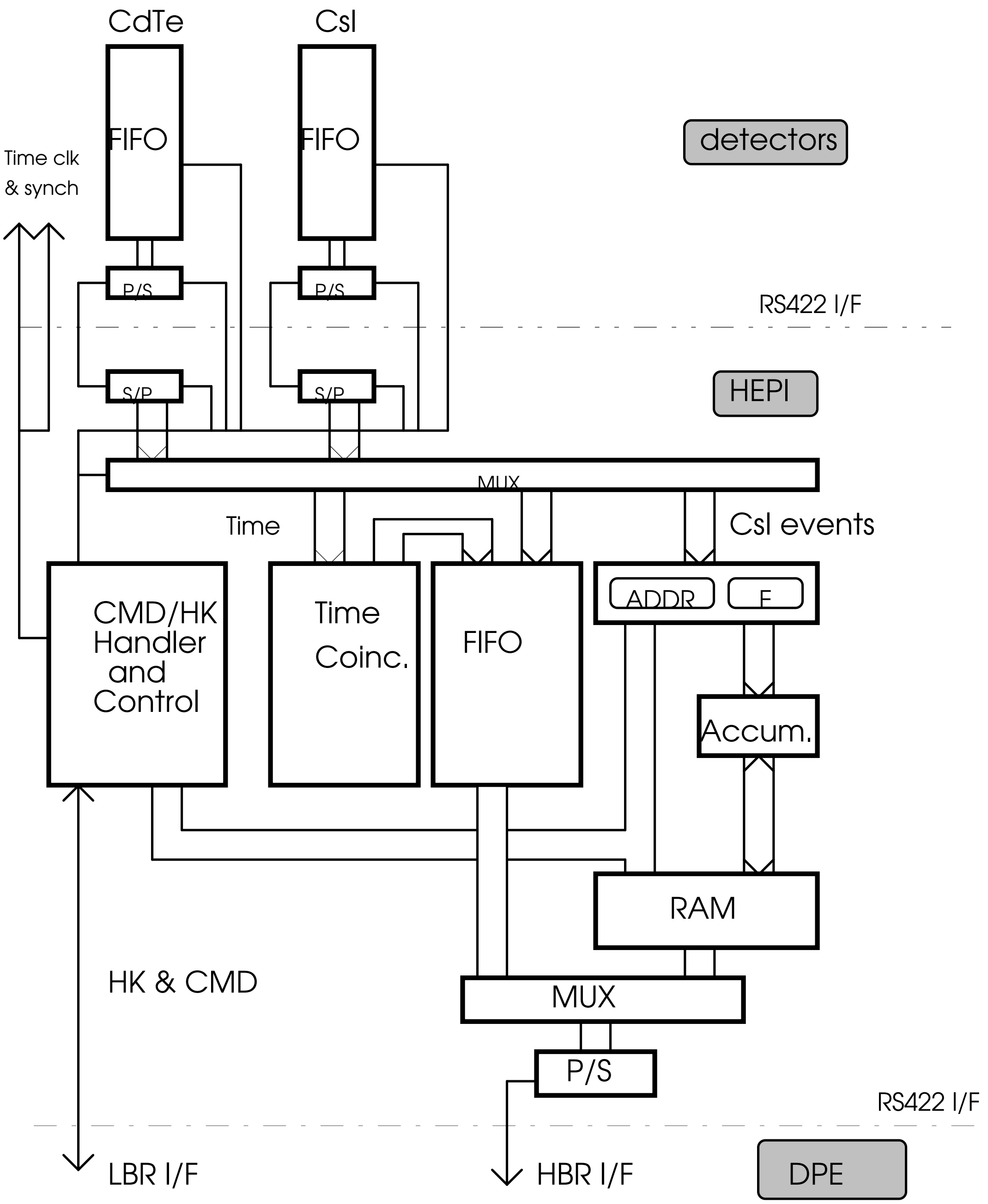

Figure 3: Functional block diagram of HEPI