On Board Scientific Data Processing Tasks for IBIS

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1. Introduction

This is a combined and updated version of our Technical Notes "Scientific Data Processing Tasks for the INTEGRAL IMAGER" (IN-IM-TUB-TN/EL-002) and "Proposal for an Hardware Event Sorter for the IMAGER (ESI)" (IN-IM-TUB-TN/EL-003).
For our calculations we have assumed the following event rates from the detectors:

- CdTe: 2400 events/s
- CsJ: 27720 events/s (The primary event rate of 16800 events/s is increased by a factor of 1.65 due to multiple events.)

2. Data Processing Tasks

Figure 1 shows the data flow from the detectors to the SPU/DPE and indicates in round boxes the data processing tasks necessary to cope with the limited telemetry capacity asigned to IBIS.

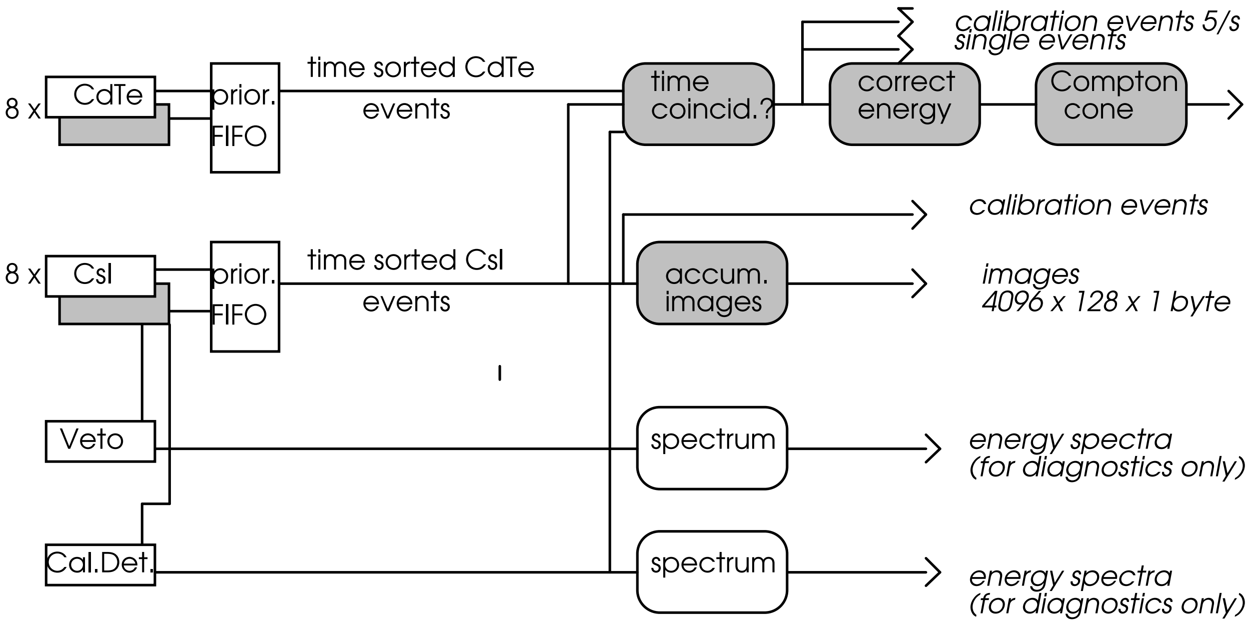

Figure 1. Data flow in DPE, filled round boxes indicate major processing tasks

3. Processing Load

We have tried to estimate the processing load for the different tasks indicated in Figure 1. Energy spectra from veto detectors and from the calibration detector will only be accumulated for diagnostic purposes. These tasks do not contribute to the processing load during normal operation. Therefore these two tasks are not further considered.

In order to estimate the processing power needed, we have written the algorithms in C language. The code then was compiled by an 68000 cross compiler and the number of assembler instructions counted. A 1750-type microprocessor (not 68000) will be used and the high level language used will be ADA (not C) therefore the results can only be taken as a first order estimate.
A more detailed analysis of the processing load is given by Martin Mohan in his report IN-IM-TUB-RP/EL-001.

Table 1: Computing load for DPE

Description of task	instructions/ event	events/s	computing load in MIPS
search event data for time coincidences CdTe- CsI	184	2400	0.44
correct energy of Compton CdTe events	40 [1)]	1200	0.05
compute Compton cone for CsI/CdTe events	80 [1)]	1200	0.10
accumulate CsI images, including handling of multiple events	44	27720	1.22
miscellanenous	40 [1)]	2400	0.10
subtotal of scientific processing			*1.91*
handling of OBDH interfaces (CMDs and data packetizing)			0.20
total processing load	-	-	2.11

Remarks:

1): Only very preliminary assumption, real algorithm not yet defined. We propose to use look-up tables in order to reduce computing time, if necessary.

The required total processing load is much higher than the available processing capability of the baseline DPE which is of the order of 1.4 MIPs. The situation becomes even worse, if one applies margins to these figures as required by the INTEGRAL Software Requirement Document (SRD). Margins of 1.33 and 2.0 are required during phase B for scientific processing and for data management tasks, respectively. Including those margins a computing capability of the DPE of 2.95 MIPs would be required, which is a factor of 2.1 above the current baseline, so we have a severe problem.

4. Possible Solutions

In principle there are three solutions to this problem.

-_We convince ourselves that the actual event rates are much lower, i.e. by more than a factor 2! *(seems to be unlikely)*

- ESTEC goes for a more powerful processor for the DPE, i.e more than a factor 2! *(seems to be unlikely)*

- Some of the tasks are performed by a dedicated hardware *(this should be possible)*

The last option is described in some detail below.

5. Proposal for a Hardware Event Preprocessor for IBIS (HEPI)

A ”Hardware Event Preprocessor” (HEPI) could perform the following tasks:

- collect event data from CdTe and CsI detectors (It is assumed that the events are sorted in time by layer.)
- search event data for time coincidences CdTe - CsI
- reconstruct multiple CsI events
- accumulate CsI images for fraction of energy range
- send event data and accumulated images to DPE
- *distribute time clock and time synch to all MCEs.*

If all multiple CsI event would be reconstructed by hardware and if for 50% of all CsI events HEPI would accumulate images, we could significantly reduce the computing load for the DPE from 2.11 MIPs to 0.82 MIPs (*1.22 MIPs including margins*), see Tab. 2.

Table 2: Computing load for DPE processor with a hardware preprocessor

Description of task	instructions/ event	events/s	computing load in MIPS
search event data for time coincidences CdTe- CsI	184	2400	N.A.
correct energy of Compton CdTe events	40 [1)]	1200	0.05
compute Compton cone for CsI/CdTe events	80 [1)]	1200	0.10
accumulate CsI images for 50% of events **excluding** handling of multiple events	44	8400	0.37
miscellanenous	40 [1)]	2400	0.10
(subtotal of scientific processing			*0.62)*
handling of OBDH interfaces (CMDs and data packetizing)			0.20
total processing load	-	-	0.82

All the required hardware could be built on one board (>100 x 160mm^2), and would consume 2-3 Watts @ 5V (TBC). All connections to the DPE would only be via standard fast and slow serial interfaces, i.e. HEPI would have no direct access to the DPE bus.
In order to keep interfaces clean and to simplify AIV activities, this board should be housed inside the DPE box and should be powered from the DPE.

Figure 1 shows a simplified block diagram of HEPI.
Event data from the detectors are read via serial interfaces to the preprocessor. After flagging time coincident events and further processing (reconstruction of multiple CsI events, accumulation of images), data are written to DPE via the two standard high bit rate interfaces. The preprocessor can be commanded through a standard low bit rate interface. This interface is also used to send HK information (status of HEPI) to the DPE.

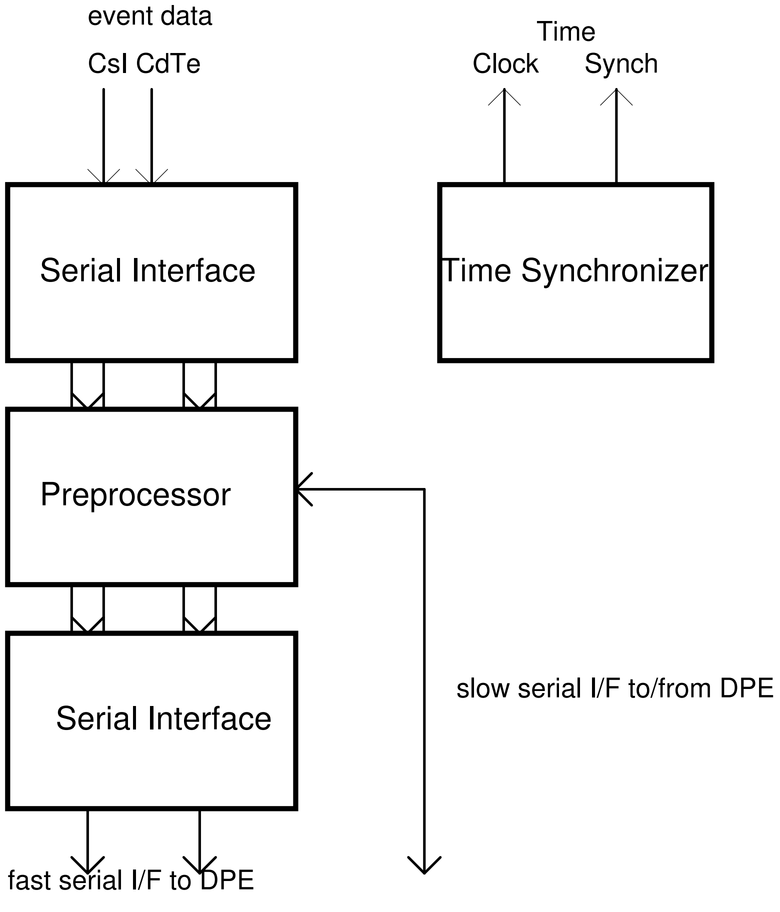

Figure 2: Block diagram of HEPI

In Figure 2 the functional blocks of the preprocessor are shown. The functioning of HEPI is controlled by registers, which are set through the slow serial interface. Data are read from the detectors and times are searched for coincidences. CdTe events which coincide with CsI events are flagged before they are written to an output FIFO. CsI events with energies within a selectable range are accumulated to event maps in an 512 kbyte RAM (TBC). The content of this RAM can be dumped to DPE on command.

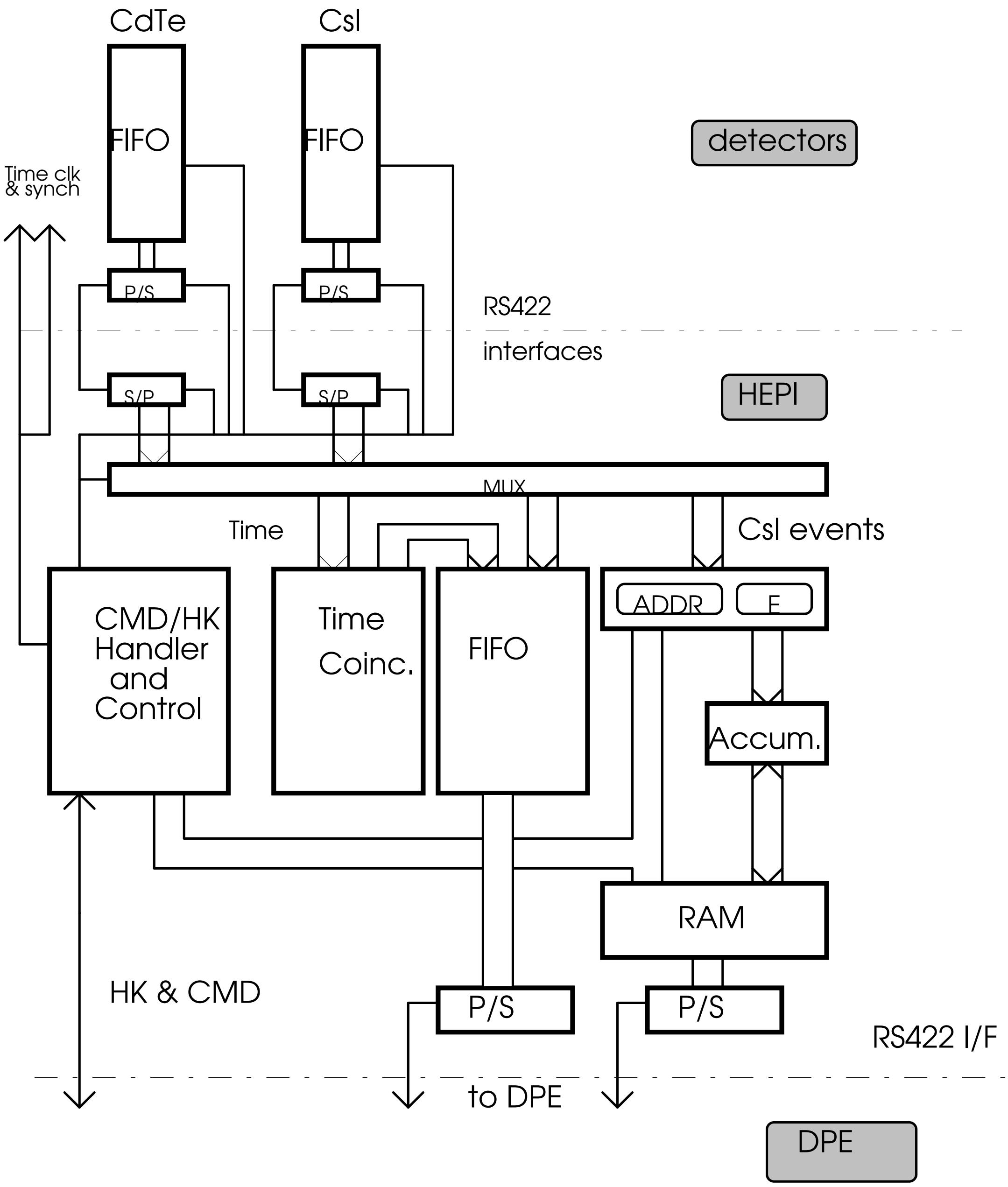

Figure 3: Functional block diagram of HEPI

6. Data Formats

In order to simplify the hardware and the onboard software, we strongly request, that event data from the detectors are transmitted to DPE (via HEPI) in a common format. To stimulate further discussions within the collaboration we propose the following format:

Event data should be transmitted as four 16 bit words.

1. word: Time in units of 250 ns (*most significant 16 bit of 24 bit time word*)
2. word: 8 bit Time (*least significant 8 bit of 24 bit time word*) plus
   8 bit Rise Time (*only applicable for CdTe, 7 bits*)
3. word: Energy (*CdTe 11 bits, CsI 10 bits*)
4. word: Pixel Address (*CdTe 14 bits, CsI 12 bits*)

Detailed bit allocation (TBD):

1. word

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

2. word

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

3. word

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

4. word

MSB															LSB
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Data should be right justified, i.e. LSB of information should be LSB of 16 bit word.
The MSB should be transmitted first.

Only prior to transmission to groud data will be packed in a more compressed format in order to save telemetry.